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THESIS

A CMOS VLSI IC
FOR REAL-TIME OPTO-ELECTRONIC
TWO-DIMENSIONAL HISTOGRAM GENERATION

by

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December, 1993

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Histogram generation, a standard image processing operation, is a record of the intensity distribution in the image. Histogram generation has straight forward implementations on digital computers using high level languages. A prototype of an optical-electronic histogram generator has been designed and tested for 1-D objects using wirewrapped MSI TTL components. The system has shown to be fairly modular in design. The aspects of the extension to two dimensions and the VLSI implementation of this design are discussed.

In this paper, we report a VLSI design to be used in a two-dimensional real-time histogram generation scheme. The overall system design is such that the electronic signal obtained from the optically scanned two-dimensional semi-opaque image is processed and displayed within a period of one cycle of the scanning process.

Specifically, in the VLSI implementation of the two-dimensional histogram generator, modifications were made to the original design. For the two-dimensional application, the output controller was analyzed as a finite state machine. The process used to describe the required timing signals and translate them to a VLSI finite state machine using Computer Aided Design Tools is discussed. In addition, the circuitry for sampling, binning, and display have been combined with the timing circuitry on one IC. In the original design, the pulse width of the electronically sampled photodetector is limited with an analog one-shot. The high sampling rates associated with the extension to two dimensions requires significant reduction in the original 1-D prototype's sample pulse width of approximately 75 ns. The alternate design using VLSI logic gates will provide one-shot pulse widths of approximately 3 ns.

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TWO-DIMENSIONAL HISTOGRAM GENERATION

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ABSTRACT

Histogram generation, a standard image processing operation, is a record of the intensity distribution in the image. Histogram generation has straight forward implementations on digital computers using high level languages. A prototype of an optical-electronic histogram generator has been designed and tested for 1-D objects using wirewrapped MSI TTL components. The system has shown to be fairly modular in design. The aspects of the extension to two dimensions and the VLSI implementation of this design are discussed.

In this paper, we report a VLSI design to be used in a two-dimensional real-time histogram generation scheme. The overall system design is such that the electronic signal obtained from the optically scanned two-dimensional semi-opaque image is processed and displayed within a period of one cycle of the scanning process.

Specifically, in the VLSI implementation of the two-dimensional histogram generator, modifications were made to the original design. For the two-dimensional application, the output controller was analyzed as a finite state machine. The process used to describe the required timing signals and translate them to a VLSI finite state machine using Computer Aided Design Tools is discussed. In addition, the circuitry for sampling, binning, and display have been combined with the timing circuitry on one IC. In the original design, the pulse width of the electronically sampled photodetector is limited with an analog one-shot. The high sampling rates associated with the extension to two dimensions requires significant reduction in the original 1-D prototype's sample pulse width of approximately 75 ns. The alternate design using VLSI logic gates will provide one-shot pulse widths of approximately 3 ns.

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I. INTRODUCTION

A. THEORY OF OPERATION

Histogram generation, a fairly standard digital image processing operation, is a record of the intensity distribution in an image [Ref. 1]. Histogram generation can be implemented on a digital computer using a high level language. However, it is generally recognized that certain operations can only be implemented in real time by not relying on the computational power of digital computers. For example, the Fourier Transform [Ref. 2] and the Hough Transform [Ref. 3] have such restrictions. Another real time example is the alternative scheme developed for nonlinear image processing operators using a hybrid optical implementation [Ref. 4].

The development of a system capable of producing a real-time histogram is of current interest since it will speed up the computationally intensive process of histogram generation through testing, comparing, and subsequent binning of values using a standard digital computer. The design of the CMOS VLSI IC that will actually perform this process is such that the electronic signal obtained from the optically scanned image is processed within a time period of one cycle of the scanning process. A one-dimensional version of this circuit has been built and tested using TTL MSI components [Ref. 5].

B. OVERVIEW OF SYSTEM DESIGN

Figure 1 shows an overview of the entire system. A semi-opaque object is sequentially scanned by a narrow beam of laser light. The transmitted light is focused on a photodetector. The electronic signal obtained from this detector is directly proportional to the transmittance of the semi-opaque object. This analog signal is used as an input to

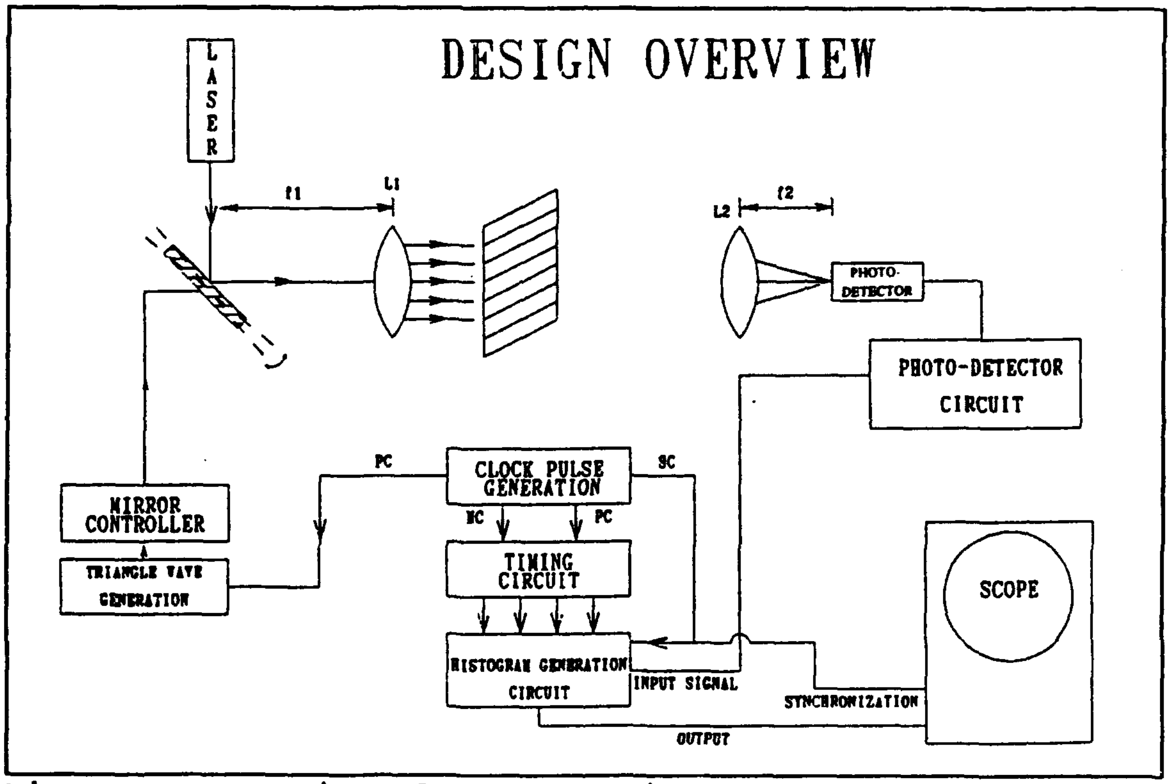


Figure 1: Overview of System Design

the histogram generation circuit. [Ref. 5]

The histogram generation circuit is where the major part of the signal processing is accomplished. Figure 2 provides

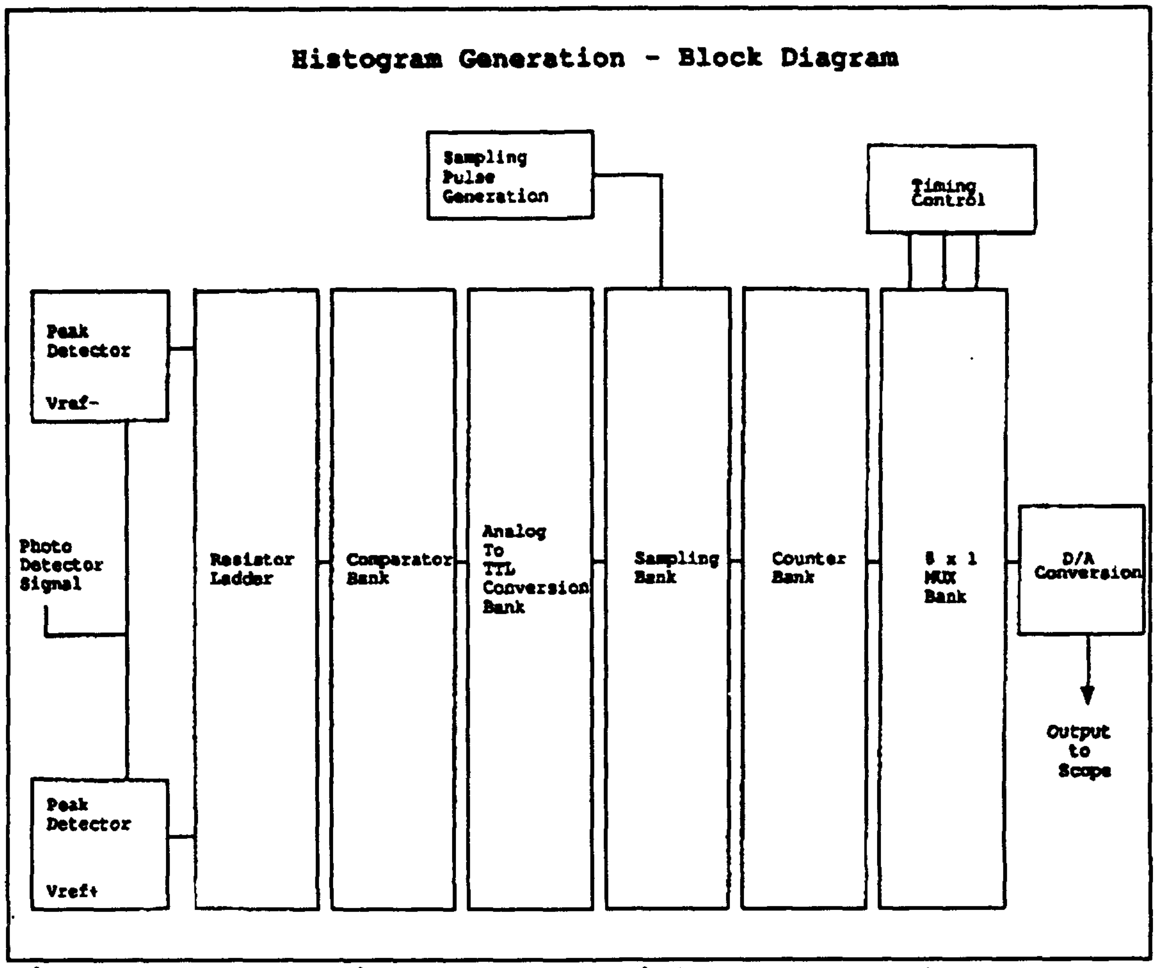


Figure 2: Block Diagram of the Histogram Generator

a block diagram of the functional blocks of this circuit. The signal from the photodetector is used as an input to both maximum and minimum peak detectors. The peak detectors are then followed by a resistor ladder which defines the boundaries of the electronic bins. The voltages obtained from the resistor ladder nodes are compared with the buffered signal from the photodetector. The output of the comparators then determine which electronic bin the photodetector signal falls into.

To facilitate further processing, the analog signals are converted to TTL voltage levels. After conversion to TTL voltage levels, it is possible to generate a TTL high on the one line corresponding to the electronic bin of the photodetector voltage.

The process of storing the information is done with a bank of counters as shown in Figure 2. Upon completion of data gathering, accomplished in the first half of the scan cycle, a bank of multiplexers is used to access the information. By proper sequencing of signals, the information from a specific counter can be multiplexed out for conversion to analog signals using a D-to-A converter.

C. RESEARCH GOALS

To accomplish real-time histogram generation, several functions of the complete circuit have been designed, developed, and implemented using CMOS VLSI. Figure 3 shows a block diagram of these functions. The integrated circuit (IC) provides 12 electronic bins vice eight in the one-dimensional design [Ref. 5] for increased signal resolution. Counter design allows for a maximum sample size of $2^{16} = 65,536$ samples. If this is the result of a two-dimensional scan of an object, an object "size" of 256 x 256 will be obtained.

The timing signals for control of the output multiplexers have been incorporated into the design since there will be a fixed number of electronic bins. Simulations of the

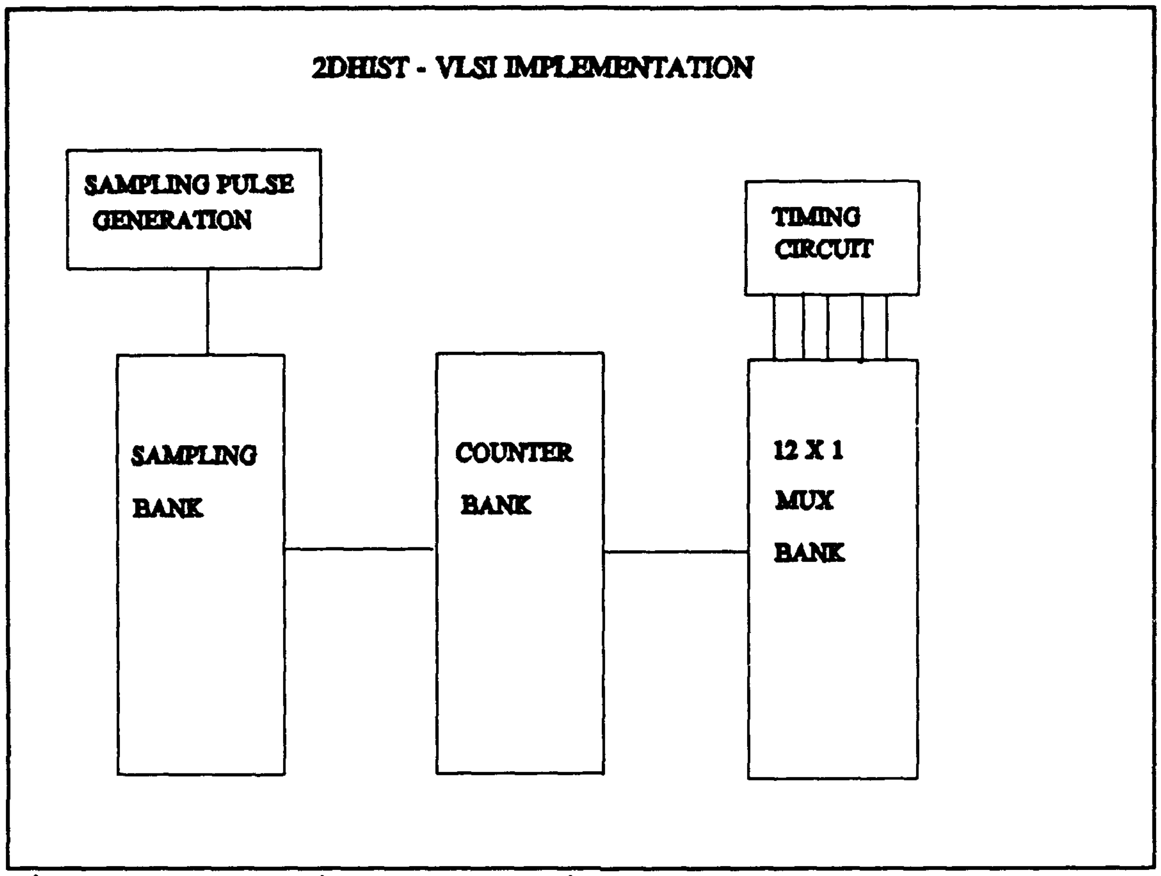


Figure 3: *Functional Block Diagram of 2DHIST*

histogram-generator have been accomplished to verify proper functional operation and to confirm layout for chip fabrication.

D. REQUIRED HARDWARE AND SOFTWARE TOOLS

The design and layout of the Two-Dimensional Histogram Generation chip was done on the Naval Postgraduate School's Sun SPARCstations utilizing the VLSI CAD tool package created by the University of California at Berkeley.

1. Sun SPARCstation

The Sun Microsystems SPARCstation II is a desktop computer that offers high-speed color graphics. Operating at 40-Mhz, the system is equipped with 32 MB of RAM, 424 MB of internal fixed disk storage, and mounts several large file systems from a remote server.

2. Magic

Magic is an interactive editor for creation of Very Large Scale Integration (VLSI) circuit layouts. This program runs on many Unix based systems, for example, the Sun SPARCstation with an integrated color display. Using Magic, the designer can create basic cell layouts, and combine them into larger structures, or even complete integrated circuit layouts. This program has a built in design rule checker that constantly checks layouts during creation to ensure that layout rules are obeyed for the particular technology being used. To allow a means of interfacing with other programs, Magic allows the user to extract the created circuits for use by other programs. Magic only permits Manhattan designs, which are designs whose edges are horizontal or vertical, no diagonal or curved structures are allowed. The further attributes of Magic are numerous and reference to the users manual is recommended for additional descriptions of its abilities [Ref. 6].

a. *Peg*

The PLA Equation Generator compiles finite state machines to generate a working PLA. It takes a high level description of a finite state machine, and translates it into the logic equations required to implement a specific design. Peg generates logic equations that follow the Moore model of a finite state machine. This implies that the outputs generated by the finite state machine depend only on the current state of the machine. Inputs can be provided to cause transitions to specific states. The equations generated by Peg are in a format compatible with the Eqntott program. For this specific finite state machine, the Peg command used was:

```
peg -s -t infile > outfile
```

This allowed for the infile, which in this case was fsm.peg, to be processed into a truth table for the fsm, and summary information to be created in a peg.summary file. Included in Appendix A. are copies of the finite state machine program, and its output fsm.out. [Ref. 6]

b. *Eqntott*

Eqntott is a generator that takes the Boolean equations generated by other programs or through operator entry and creates a truth table. From this truth table, other functions such as logic minimization and PLA generation can be accomplished. Through various options, the output variables can be made in various ways. The option chosen for this work was the -l option in which the input and output variables are mutually exclusive. Also, a truth table is generated that is compatible with the Espresso program used to minimize logic functions. The command used was:

```
eqntott -l infile > outfile
```

The infile was fsm.out and the outfile was fsm.eqn, these outputs may be seen in Appendix A. [Ref. 6]

c. Espresso

Espresso is program that performs minimization of a Boolean logic function. The input and output of espresso are in the form of a truth table and compatible with the format required to generate a Programmable Logic Array (PLA). The command used was:

```
espresso infile > outfile
```

The infile was fsm.eqn and the outfile was fsm.esp, these outputs may be seen in Appendix A. [Ref. 6]

d. Mpla

Mpla is a PLA generator that can generate Magic layout compatible PLAs in various styles and technologies. There are several styles of PLAs that are supported by this program. This work was completed in scalable CMOS cis version (SCS3cis). It supports MOSIS 1.5/2.0/3.0 micron SCMOS processes, a pseudo-NMOS static PLA with p-channel pullups, clocked inputs, and clocked outputs if required. The cis stands for buried contacts, with inputs and outputs on the same side of the PLA. Also available was SCS3trans, which is the same except the inputs and outputs are on opposite sides of the PLA. A dynamic PLA style is also provided called SCD3cis or SCD3trans.

The Two-Dimensional Histogram Generation timing control finite state machine (PLA) was generated using standard inputs and outputs since one of the inputs is a clock. The command used to generate the PLA was:

```
mpla -s SCS3cis -o outfile infile
```

The infile was fsm.esp and the outfile was fsm.mag. The completed PLA was generated with some design rule violations requiring manual correction. These errors are generated by the design tool Mpla and are not caused by user error. The finite state machine PLA also required the addition of flip-flops for state storage. A plot of the finished finite state machine can be seen in Appendix B. Figure 27. [Ref. 6]

e. *SPICE3C1*

SPICE3C1 is an updated version of SPICE which is a general purpose circuit simulation program. It can perform dc analysis, ac small-signal analysis, and transient analysis. SPICE can also be used to provide extensive plotting of circuit parameters and circuit behavior using its plot command. SPICE is a tremendously powerful tool in observing how circuits are acting, but it has a limitation in that large circuits take an extremely long time to process. It was for this reason that it was used mainly for power estimations and transient behavior. Esim was used for logic simulations. [Ref. 7]

f. *Esim*

Esim is an event-driven switch-level simulator for NMOS and CMOS circuits. It can be entered after the circuit has been extracted in Magic. Esim is used to watch various nodes, to set or reset nodes, and to simulate the logical operation of the circuit. The watched nodes can then be inspected, and the circuit evaluated. There are numerous commands and options that may be employed in the simulation, and the reader is directed to the reference material for further clarification. [Ref. 6]

E. THESIS STRUCTURE

The fundamental block designs are discussed in chapter II. The implementation and basic descriptions along with electronic parameters are shown in chapter III. Simulations of the finite state machine and the complete circuit will be presented in chapter IV. Chapter V outlines the thesis conclusions and further recommendations.

II. TWO-DIMENSIONAL HISTOGRAM GENERATOR DESIGN

In order to implement the Two-dimensional Histogram Generator, several functional blocks will be utilized, as shown in Figure 3.

A. SAMPLING PULSE GENERATION

Sampling pulse generation is accomplished by passing the Master Clock (MC) signal through a digital one shot. The MC is logically combined with the Scan Clock (SC) signal so that sampling is only performed during the first half of the scan cycle. The digital one shot then limits the pulse width to provide a more accurate discrete sample of the input from the photodetector.

B. SAMPLING BANK

The logic required to determine which bin will receive input is performed by the PEXAND block. The input to the IC is such that during sampling, one and only one PEXAND block will have a high output.

C. COUNTER BANK

The actual histogram generation is performed in the counter bank. Each electronic bin corresponds to a 16 bit counter that stores a count corresponding to the percentage of time that the photodetector output spent in a given voltage range. The input to the counter bank comes from the output of the PEXAND blocks.

D. MULTIPLEXER BANK

The output from the histogram generator is generated by a bank of 12-to-1 multiplexers (MUX). Each MUX output corresponds to one bit of a selected electronic bin. Each MUX will output a signal to be converted from digital-to-analog and displayed on an oscilloscope.

E. TIMING CIRCUIT

The control signals required to operate the bank of MUXs comes from a finite state machine. The finite state machine provides the following signals:

- MUXEN - an enable signal to allow the MUX's to output for Digital to Analog conversion and display.
- CLEAR - a signal to reset the bank of counters used for data acquisition.
- S3,S2,S1,S0 - the control signals required to select which electronic bin will be presented for data conversion.

F. 2DHIST OVERALL CHIP LAYOUT

Figure 4 is a floor plan of the two-dimensional histogram generation IC showing the overall layout of the major cells. For simplicity, the required cell interconnects and input and output pads have been omitted. Detailed Magic cell layouts

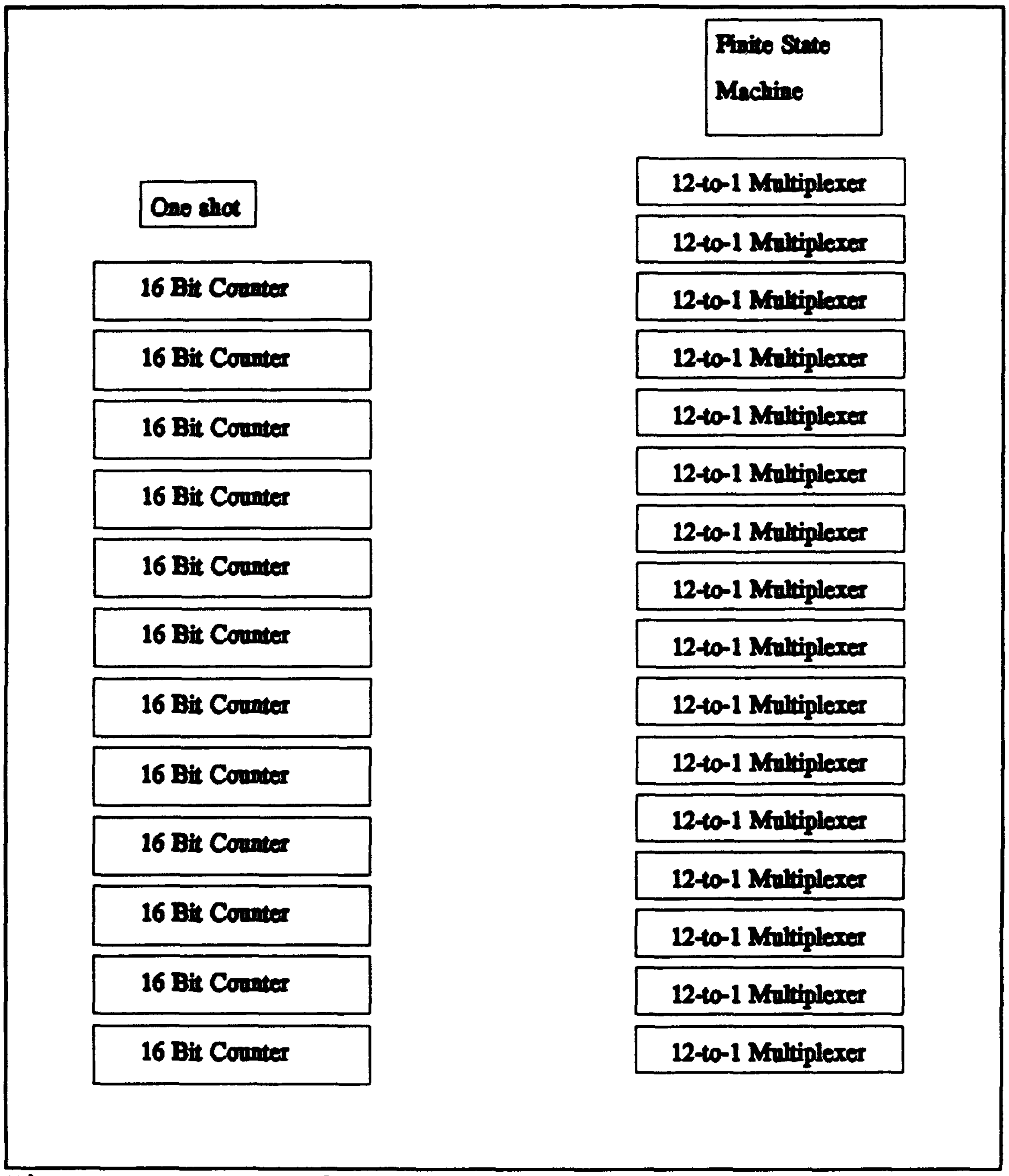


Figure 4. 2DHIST Floor Plan

are provided in Appendix B.

III. IMPLEMENTATION

The basic logic design of each of the cells used in the Two-Dimensional Histogram Generator will be shown. This will provide insight into the design characteristics of each of the cells. The basic cell layouts are included in Appendix B so that the reader can see how the cell descriptions given appear in a Magic layout format.

A. CELL CONVERSION

The cell plots in the appendix were created using the Magic function cif which creates a file cell.cif. [Ref. 6] The .cif file is then converted by the routine cif2ps. In order to include these files in the thesis, further conversion to a .pcx file was needed. The following conversion is available on alioth at the computer center as follows:

```
pstoppm filename.ps ¦ imconv -ppm - -pcx filename.pcx
```

Note: This is a general conversion utility. To convert to some other standard format, replace pcx with the extension of the type of graphics you want to convert to, i.e. tiff, gif, eps, etc.

B. 16-BIT COUNTER

The 16-Bit counter is an edge-triggered ripple-counter with an asynchronous clear. The counter is built from eight

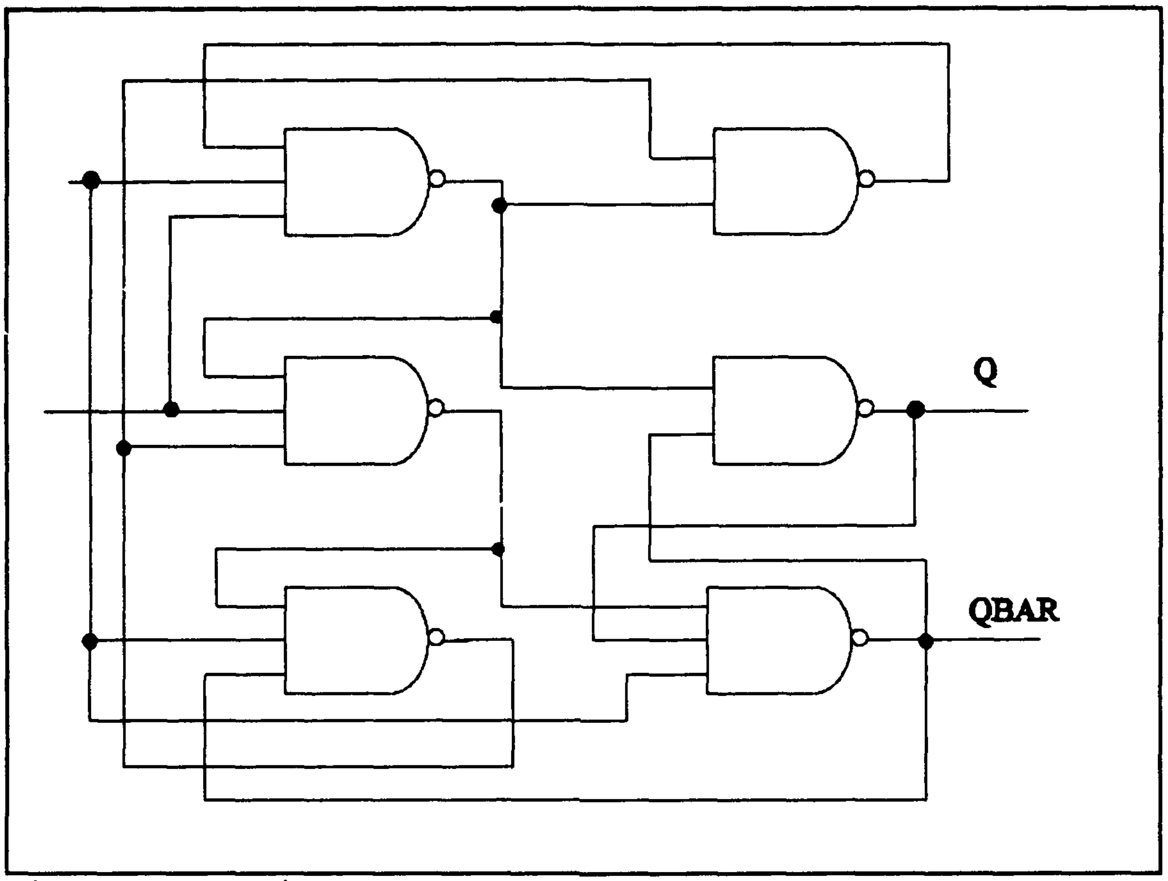


Figure 5. 1 Bit Counter

two-bit counters. Each two-bit counter is built from two one-bit counters. The one-bit counters are built from three-input and two-input NAND gates, as seen in Figure 5. The one-bit counter uses the input signal NCLR to determine whether or not the counter is enabled or in a reset condition. When NCLR = 1, the counter is enabled and when NCLR = 0, the counter is reset. The counter toggles output states each time a new clock pulse is input to the counter.

C. MULTIPLEXER CELL

The multiplexers (MUX) used in the Two-Dimensional Histogram Generator are all 12-to-1 MUXs that act like a switch, selecting one line or another depending on the state of the select lines. These particular switches are unidirectional devices that only allow data to flow from their input to their output. The twelve input lines, I0 through I11, are selected based on the values of select lines, S0 through S3. In addition, since it is desired to only have a valid output during the second portion of the scan cycle, the circuit is provided with an enable line, MUXEN. The enable line MUXEN must be a logic 1 for any of the lines to be selected. This gives the finite state machine the ability to turn the MUX on or off as needed. [Ref. 8] Table I shows the truth table for the operation of the MUX.

Table I. TRUTH TABLE FOR 12-TO-ONE MULTIPLEXER

MUXEN	S3	S2	S1	S0	OUT
0	X	X	X	X	0
1	0	0	0	0	I0
1	0	0	0	1	I1
1	0	0	1	0	I2
1	0	0	1	1	I3
1	0	1	0	0	I4
1	0	1	0	1	I5
1	0	1	1	0	I6
1	0	1	1	1	I7
1	1	0	0	0	I8
1	1	0	0	1	I9
1	1	0	1	0	I10
1	1	0	1	1	I11

X = DON'T CARE

D. ONE SHOT CELL

In order to provide a narrow pulse for sampling, the one-dimensional prototype used an analog one shot. [Ref. 5] However, in the CMOS implementation of this circuit, a digital one shot was used. The delay obtained from this circuit is based on the propagation delay time through a series of logic inverters. Figure 6 shows a diagram of the one shot cell. The output from the one shot circuit is a 0 until the rising edge of an input pulse is sensed. On the rising edge, a 1 is

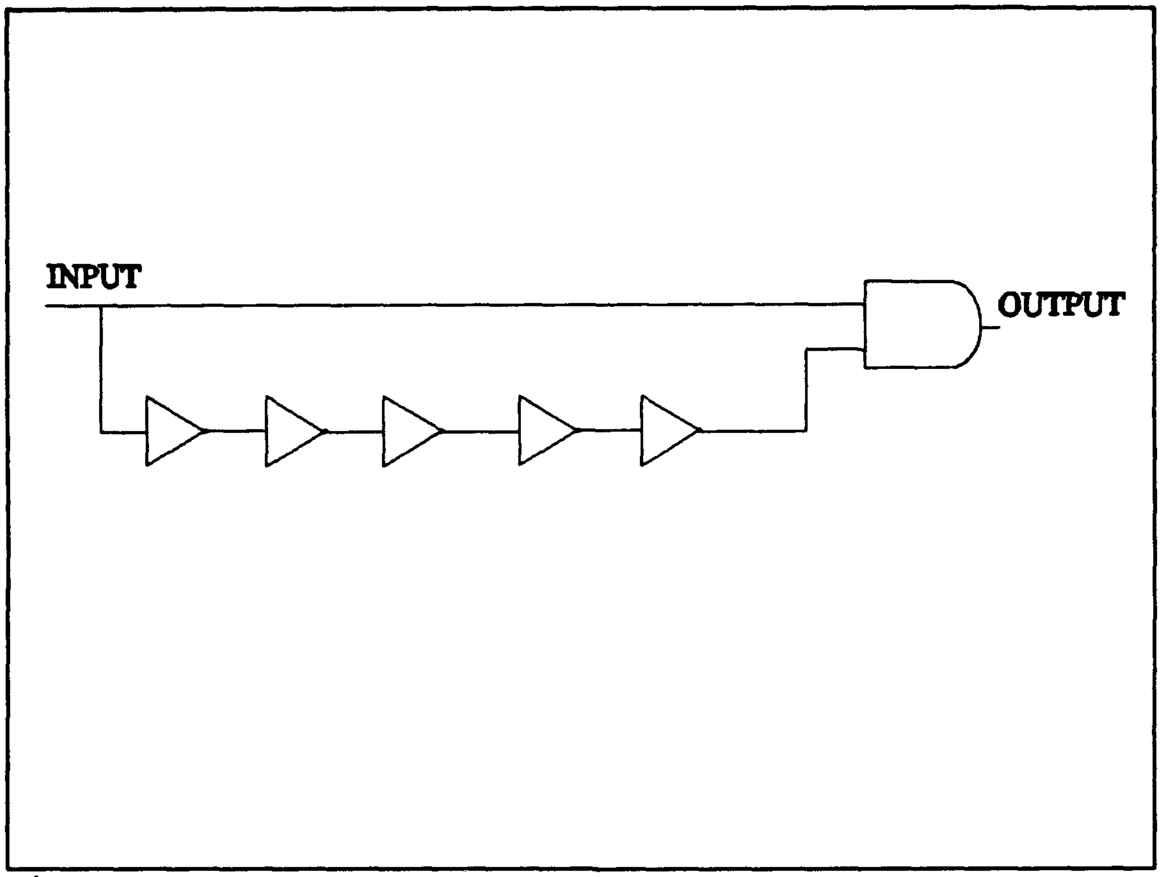


Figure 6. One Shot Cell

output until the input signal has propagated through the inverters to give an output of 0 until the next rising edge. Using SPICE31, the typical gate delay through a single inverter when transitioning from a high to a low is about 0.28ns, and the delay when transitioning from low to high is about 0.65ns. In order to ensure adequate setup time for the 16 bit counters and other logic on the IC, it was decided to use five inverters in the initial design.

Using five inverters in series will give a predicted delay through the inverters of about 2.19ns. This is calculated as shown in (1).

$$T_{delay} = 3*Tprop_{HL} + 2*Tprop_{LH} \qquad (1)$$

Using this pulse width and allowing for about 0.33ns extra for rise and fall of the input pulse should allow a maximum Master Clock frequency of about 300Mhz.

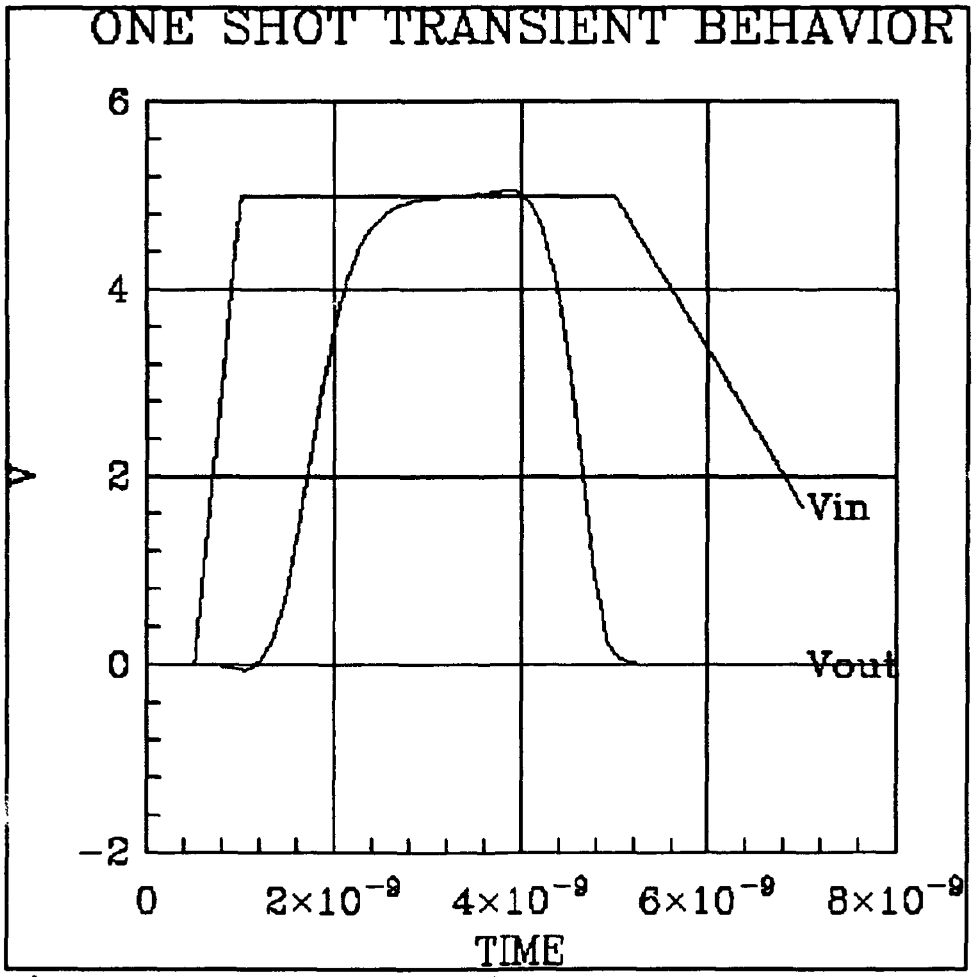


Figure 7. One Shot Transient Response

Figure 7 is a plot of transient response using Spice. From this simulation, the one shot pulse width, including the delay through the and gate, will be approximately 3ns. This compares well with the predicted pulse width using each individual component.

E. FINITE STATE MACHINE

In the original design, the timing control function was furnished by an N-and-only-N pulse generator. [Ref. 5] Figure 8 shows a block diagram of the timing control circuitry used in the one dimensional design. The purpose of this circuit is to generate the signals S0, S1, S2 and S3 used to control output from the histogram circuit. In addition, signals need to be generated in the two dimensional design to enable the output from the multiplexers and to reset the counters. In the one dimensional design, these signals were generated from S0, S1, S2 and S3 using combinational logic.

In the two dimensional design, these signals will be incorporated into the required outputs from the finite state machine. Figure 9 shows a timing diagram for the relevant signals generated by the timing circuit in the one-dimensional case. In addition, timing signals for the scan clock (SC) and scan pulses (SP) are shown.

These signals were used to define the required states for implementing a simple finite state machine. For the two-dimensional histogram generator, fourteen states are required

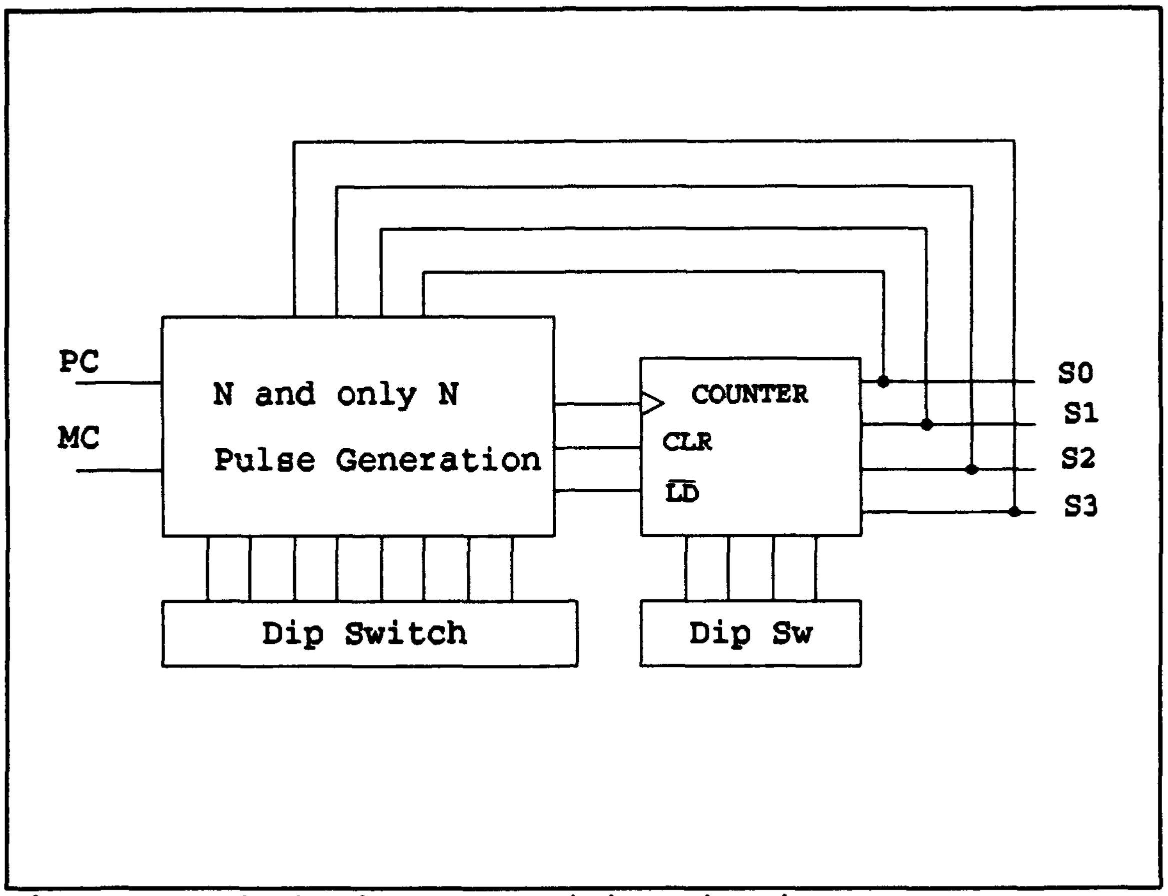


Figure 8. Block Diagram of Timing Circuit - 1D case

to provide control signals, as illustrated in Figure 10. From the states defined in Figure 10, Table II was developed to define the required outputs for each state. A PEG program was then written for the PLA generator CAD tool PEG using the data from Table II. (See Appendix A.) The PEG program defines the inputs, outputs, and states for a finite state machine. The program is executed by the PEG generator to create the logic equations that describe the desired finite state machine. The logic equations generated by PEG are in a format that can be input into another CAD program EQNTOTT.

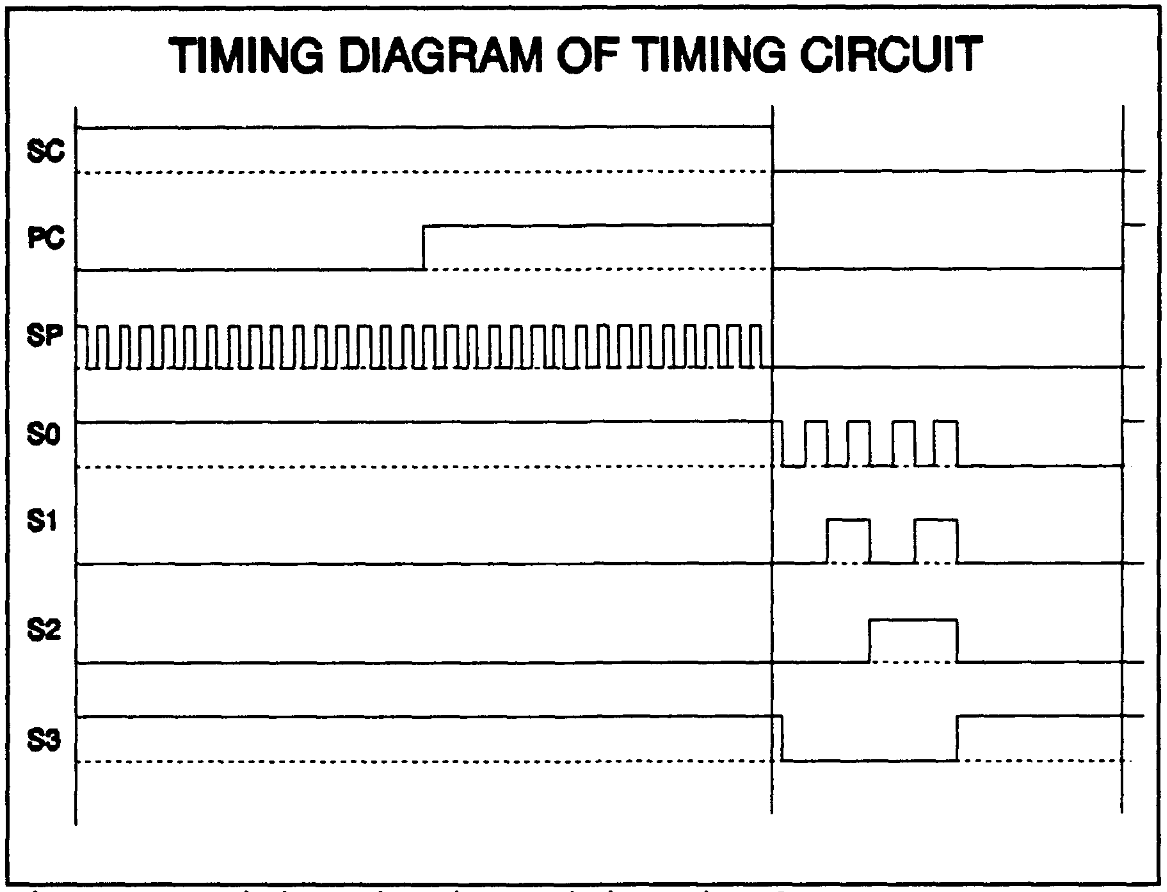


Figure 9. Timing Circuit - Timing Signals - 1D case

Eqntott generates a truth table representation of the PEG program from a set of boolean equations which define the PLA outputs in terms of the inputs. (See Appendix A.) This input is then sent to a logic minimization program called ESPRESSO.

Espresso performs a logic minimization for a boolean expression input in the form of a truth table. Espresso generates a minimized truth table representation of the EQNTOTT truth table. (See Appendix A.)

This output is then sent to the MPLA program which is a PLA generator that generates a PLA in several different styles and technologies. The technology selected for this work was

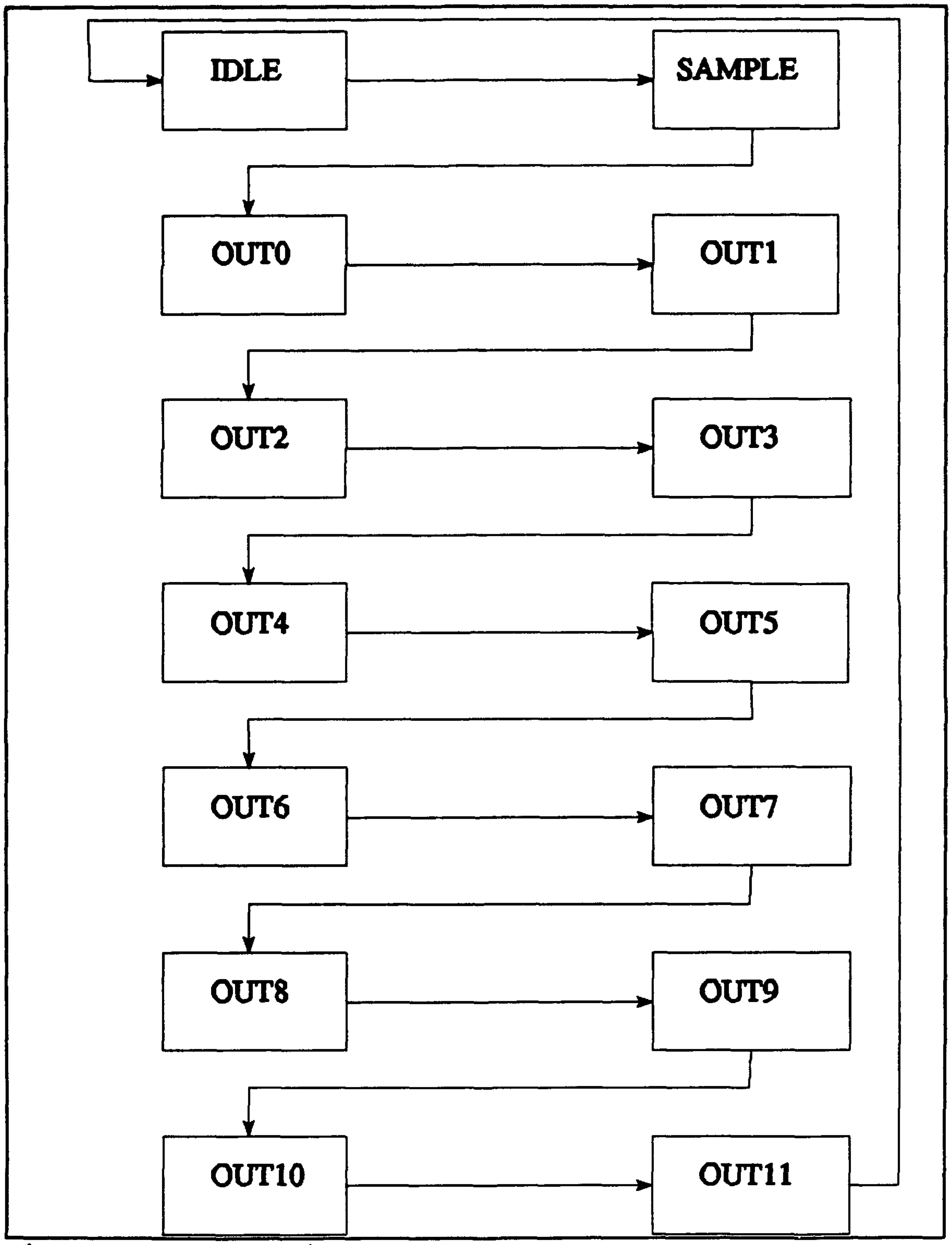


Figure 10. State Diagram for FSM

scalable CMOS cis version. (See Mpla section I.D.2.d.) From

Table II. TRUTH TABLE FOR THE TWO-DIMENSIONAL FSM

STATE	S3	S2	S1	S0	MUXEN	CLEAR
IDLE	0	0	0	0	0	0
SAMPLE	0	0	0	0	0	1
OUT0	0	0	0	0	1	1
OUT1	0	0	0	1	1	1
OUT2	0	0	1	0	1	1
OUT3	0	0	1	1	1	1
OUT4	0	1	0	0	1	1
OUT5	0	1	0	1	1	1
OUT6	0	1	1	0	1	1
OUT7	0	1	1	1	1	1
OUT8	1	0	0	0	1	1
OUT9	1	0	0	1	1	1
OUT10	1	0	1	0	1	1
OUT11	1	0	1	1	1	1

this, a MAGIC layout was produced that could be slightly modified to obtain the final working layout that can be viewed in Appendix B. Some work was required on the output of MPLA, such as correcting various design rule violations created by the MPLA program, and connecting flip-flops for state storage. Since each of the outputs will be required to drive many MUXs, buffers were added to each of the outputs to improve fanout from the finite state machine.

F. POWER ESTIMATES

Electromigration refers to the transport of metal ions through a conductor that results from excessive current density in the conductor. In determining the minimum size for conductors, especially power and ground, it is necessary to estimate the current density of the conductor. If the current density is too high, this can lead to a weakening of the conductor, which eventually blows like a fuse. [Ref. 9]

SPICE3C1, a general-purpose circuit simulation program that provides dc and ac analyses, was used to determine the power consumption of each circuit. [Ref. 7]

1. Static Power Dissipation

The static power consumption is defined as worst-case leakage current multiplied by Vdd in any specific device. The results for each of the building blocks for the two-dimensional histogram generator are shown in Table II.

The total static dissipated power (Worst Case) can be found by multiplying the value in Table II by the total number of each gate. The Total value is estimated to be 9.5mW. This assumes that all gates are in their worst case steady-state value.

Table III. STATIC POWER CONSUMPTION

CELL	CELL POWER	No. of CELLS	TOTAL
PNAND2	69.3pW	384	26.61nW
PNAND3	104pW	768	79.8nW
PNAND4	138.65pW	48	6.65nW
NAND5	173.35pW	192	33.3nW
PAND	104pW	30	3.12nW
BUFFER4X-8X	69.35pW	99	6.86nW
BUFFER1X-4X	69.35pW	24	1.66nW
PINV	34.665pW	5	173.3pW
PEXOR	200.15pW	12	2.4nW
PINVX4	34.665pW	64	2.2nW
POR3	138.65pW	16	2.2nW
STATE	9.5mW	1	9.5mW
TOTAL			9.5mW

2. Dynamic Power Consumption

The dynamic power consumption is defined as the current during a device's transition multiplied by Vdd. The total dynamic power consumption can then be estimated by multiplying this value by the amount of each device used. The results for each of the building blocks for the two-dimensional histogram generator are shown in Table IV.

The total dynamic dissipated power (Worst Case) can be found by multiplying the value in Table IV by the total number of each gate. The total value is estimated in two parts, the

Table IV. DYNAMIC POWER CONSUMPTION

CIRCUIT	IND PWR	NUMBER	SC=1	SC=0
PNAND2	408µW	384	156.7mW	--
PNAND3	935µW	768	718mW	--
PNAND4	667µW	48	--	32mW
NAND5	724µW	192	--	139mW
PAND	735µW	30	10mW	11.8mW
BUFFER1X-4X	1.5mW	24	36mW	--
BUFFER4X-8X	3.8mW	99	49.4mW	326.8mW
PINV	378µW	5	1.89mW	--
PEXOR	378µW	12	4.5mW	--
PINVX4	1.1mW	64	--	70.4mW
POR3	766µW	16	--	12mW
STATE		1	--	13.5mW
TOTALS	--	--	976.5mW	605.5mW

first part is the portion of the scan cycle for sampling and the second portion is for output. During the first part, the maximum estimated total dynamic power is 976.5mW. During the second part, the maximum estimated total dynamic power is 605.5mW.

IV. SIMULATIONS

All magic cells were simulated using the event driven logic-level simulator Esim. Each major cell building block, e.g. 2-bit counter, 12-to-1 multiplexer, and the finite state machine were simulated to verify performance of their required functions. In addition, to determine the resultant pulse width and delay for the one shot, Spice was used to perform a transient analysis. To avoid redundancy of simulation results, only the results for the finite state machine, the one shot, and the entire chip will be presented.

A. FINITE STATE MACHINE TESTING

For the finite state machine to operate properly, two inputs are required. A clock signal to control the transition between states and the Scan Clock (SC). The SC signal determines whether or not the finite state machine is idle. During the sampling half of the cycle, the finite state machine outputs a signal that allows the counters to count. During the output half of the cycle, the finite state machine outputs signals that enable the multiplexers and step through each bin for output to an oscilloscope. Appendix C part A shows the test vectors and results for the simulation of the finite state machine.

B. ONE SHOT TESTING

The one shot could not be adequately tested using the event driven simulator Esim. Esim was only able to show the final state achieved during each clock cycle, not the transient behavior during the clock period. To show the transient behavior, Spice was used to view the behavior during a single clock cycle. Figure 7 contains a plot of the transient analysis. From the transient analysis, the approximate pulse width of the one shot is 3ns.

C. 2DHIST TESTING

The testing of the entire two-dimensional histogram generation circuit required that the Scan Clock, Master Clock, and comparator outputs all be simulated as inputs in order to ensure the internal performance of the 2DHIST. To verify proper operation of the circuit, many data runs were accomplished to ensure that when data is applied, only one bin receives data for a given simulation and data is output properly. Appendix C part C presents the multiple simulations performed to ensure proper chip operation.

It is important to note that each simulation is run twice. The finite state machine used to control the circuit is self-starting. The first test cycle after power-on contains erroneous data as the process is initialized. However, on the second and subsequent cycles, all results are accurate.

V. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

1) The two-dimensional histogram generation circuit has been designed to be implemented on a single chip. Although the 2DHIST uses a standard CMOS process, the functionality is a new contribution to opto-electronic system technology.

2) Further testing or simulation is required in a working system to determine the actual size and performance gains from this circuit.

B. RECOMMENDATIONS

1) Design and build a controller to control the mirror and analog portions of the circuit on a single chip.

2) Put the 2DHIST in an actual circuit and test it out.

APPENDIX A: FINITE STATE MACHINE DESIGN

A. PEG PROGRAM FOR FSM

```
INPUTS: SC;
OUTPUTS: S3,S2,S1,S0,MUX_EN, CLEAR;
IDLE:      if  SC then SAMPLE else IDLE;
SAMPLE:    assert CLEAR;
        if  SC  then SAMPLE else OUT0;
OUT0:      assert MUX_EN,CLEAR;
        if NOT SC then OUT1 else IDLE;
OUT1:      assert S0,MUX_EN,CLEAR;
        if NOT SC then OUT2 else IDLE;
OUT2:      assert S1,MUX_EN,CLEAR;
        if NOT SC then OUT3 else IDLE;
OUT3:      assert S0,S1,MUX_EN,CLEAR;
        if NOT SC then OUT4 else IDLE;
OUT4:      assert S2,MUX_EN,CLEAR;
        if NOT SC then  OUT5 else IDLE;
OUT5:      assert S0,S2,MUX_EN,CLEAR;
                if NOT SC then OUT6 else IDLE ;
OUT6:      assert S1,S2,MUX_EN,CLEAR;
        if NOT SC then OUT7 else IDLE;
OUT7:      assert S0,S1,S2,MUX_EN,CLEAR;
        if NOT SC then OUT8 else IDLE;
OUT8:      assert S3,MUX_EN,CLEAR;
            if NOT SC then OUT9 else IDLE;
OUT9:      assert S0,S3,MUX_EN,CLEAR;
                if NOT SC then OUT10 else IDLE;
OUT10:     assert S1,S3,MUX_EN,CLEAR;
                if NOT SC then OUT11 else IDLE;
OUT11:     assert S0,S1,S3,MUX_EN,CLEAR;
            GOTO IDLE;
```

B. PEG OUTPUT

```
INORDER=
   SC
   InSt0*
   InSt1*
   InSt2*
   InSt3*;
OUTORDER=
   OutSt3*
   OutSt2*
   OutSt1*
   OutSt0*
   S3
   S2
   S1
   S0
   MUX_EN
   CLEAR;
OutSt3*=
     (!SC& InSt0*&!InSt2*&!InSt3*)|
     (!SC&!InSt1*& InSt2*&!InSt3*)|
     (!SC&!InSt0*& InSt1*&!InSt3*)|
     ( SC&!InSt0*&!InSt1*&!InSt2*);
OutSt2*=
     (!SC&!InSt1*& InSt2*&!InSt3*)|
     (!SC&!InSt1*&!InSt2*& InSt3*)|
     (!SC&!InSt0*& InSt1*& InSt2*&!InSt3*)|
     (!SC&!InSt0*& InSt1*&!InSt2*& InSt3*);
OutSt1*=
     (!SC& InSt1*&!InSt2*&!InSt3*)|
     (!SC&!InSt1*& InSt2*& InSt3*)|
     (!SC&!InSt0*& InSt1*& InSt2*&!InSt3*)|
     (!SC&!InSt0*& InSt1*&!InSt2*& InSt3*);
OutSt0*=
     (!SC& InSt0*&!InSt2*&!InSt3*)|
     (!SC& InSt0*&!InSt1*& InSt2*)|
     (!SC& InSt0*&!InSt1*&!InSt2*& InSt3*)|
     (!SC&!InSt0*& InSt1*& InSt2*& InSt3*);
S3=
     ( InSt0*& InSt1*&!InSt2*)|
     ( InSt0*&!InSt1*& InSt2*);
S2=
     ( InSt0*&!InSt1*&!InSt2*)|
     (!InSt0*& InSt1*& InSt2*);
S1=
     ( InSt0*&!InSt2*)|
     (!InSt0*& InSt1*&!InSt2*);
S0=
     ( InSt0*&!InSt2*& InSt3*)|
        (!InSt1*& InSt2*& InSt3*)¦
        (!InSt0*& InSt1*& InSt3*);
MUX_EN=
        ( InSt0*&!InSt2*)¦
        (!InSt1*& InSt2*)¦
        (!InSt0*& InSt1*);
CLEAR=
        ( InSt0*&!InSt2*)¦
        (!InSt1*& InSt2*)¦
        (!InSt0*& InSt1*)¦
        (!InSt0*&!InSt1*&!InSt2*& InSt3*);
```

C. SUMMARY FROM PEG

```
SUMMARY INFORMATION GENERATED BY PEG FROM FILE fsm.peg
peg:  Number of inputs  =1
peg:  Number of outputs =6
peg:  Number of states  =14
peg:  State field size  =4 * 2
peg:  Table width       =15

INPUTS:
   i00:  SC
   s00:  InSt0* (msb)
   s01:  InSt1*
   s02:  InSt2*
   s03:  InSt3* (lsb)

OUTPUTS:
   n03:  OutSt3* (lsb)
   n02:  OutSt2*
   n01:  OutSt1*
   n00:  OutSt0* (msb)
   o00:  S3
   o01:  S2
   o02:  S1
   o03:  S0
   o04:  MUX_EN
   o05:  CLEAR

State Table
     i  s  s  s  s  n  n  n  n  o  o  o  o  o  o
     0  0  1  2  3  3  2  1  0  0  1  2  3  4  5
   ----------------------------------------------
     0  0  0  0  0  0  0  0  0  -  -  -  -  -  -    IDLE
     1  0  0  0  0  1  0  0  0  -  -  -  -  -  -    IDLE
     0  0  0  0  1  0  1  0  0  -  -  -  -  -  1    SAMPLE
     1  0  0  0  1  1  0  0  0  -  -  -  -  -  1    SAMPLE
     0  0  0  1  0  1  1  0  0  -  -  -  -  1  1    OUT0
     1  0  0  1  0  0  0  0  0  -  -  -  -  1  1    OUT0
     0  0  0  1  1  0  0  1  0  -  -  -  1  1  1    OUT1
     1  0  0  1  1  0  0  0  0  -  -  -  1  1  1    OUT1
     0  0  1  0  0  1  0  1  0  -  -  1  -  1  1    OUT2
     1  0  1  0  0  0  0  0  0  -  -  1  -  1  1    OUT2
     0  0  1  0  1  0  1  1  0  -  -  1  1  1  1    OUT3
     1  0  1  0  1  0  0  0  0  -  -  1  1  1  1    OUT3
     0  0  1  1  0  1  1  1  0  -  1  -  -  1  1    OUT4
     1  0  1  1  0  0  0  0  0  -  1  -  -  1  1    OUT4
     0  0  1  1  1  0  0  0  1  -  1  -  1  1  1    OUT5
     1  0  1  1  1  0  0  0  0  -  1  -  1  1  1    OUT5
     0  1  0  0  0  1  0  0  1  -  1  1  -  1  1    OUT6
```

```
1  1  0  0  0  0  0  0  0  -  1  1  -  1  1    OUT6
0  1  0  0  1  0  1  0  1  -  1  1  1  1  1    OUT7
1  1  0  0  1  0  0  0  0  -  1  1  1  1  1    OUT7
0  1  0  1  0  1  1  0  1  1  -  -  -  1  1    OUT8
1  1  0  1  0  0  0  0  0  1  -  -  -  1  1    OUT8
0  1  0  1  1  0  0  1  1  1  -  -  1  1  1    OUT9
1  1  0  1  1  0  0  0  0  1  -  -  1  1  1    OUT9
0  1  1  0  0  1  0  1  1  1  -  1  -  1  1    OUT10
1  1  1  0  0  0  0  0  0  1  -  1  -  1  1    OUT10
-  1  1  0  1  0  0  0  0  1  -  1  1  1  1    OUT11

------------------------------
peg:  Eliminated Vectors=79
```

D. EQNTOTT OUTPUT

```
.i 5
.o 10
.na fsm
.ilb  SC InSt0* InSt1* InSt2* InSt3*
.ob  OutSt3* OutSt2* OutSt1* OutSt0* S3 S2 S1 S0 MUX_EN CLEAR
.p 24
-0001  0 0 0 0 0 0 0 0 0 1
0-001  0 1 0 0 0 0 0 0 0 0
--01-  0 0 0 0 0 0 0 0 1 1
0-010  1 1 0 0 0 0 0 0 0 0
--011  0 0 0 0 0 0 0 1 0 0
0-011  0 0 1 0 0 0 0 0 0 0
001-0  1 0 0 0 0 0 0 0 0 0
-010-  0 0 0 0 0 0 1 0 0 0
-01--  0 0 0 0 0 0 0 0 1 1
0-100  0 0 1 0 0 0 0 0 0 0
00101  0 1 1 0 0 0 0 0 0 0
-01-1  0 0 0 0 0 0 0 1 0 0
00110  0 1 1 0 0 0 0 0 0 0
-011-  0 0 0 0 0 1 0 0 0 0
00111  0 0 0 1 0 0 0 0 0 0
-100-  0 0 0 0 0 1 0 0 0 0
01-00  1 0 0 1 0 0 0 0 0 0
-1-0-  0 0 0 0 0 0 1 0 1 1
-1-01  0 0 0 0 0 0 0 1 0 0
01001  0 0 0 1 0 0 0 0 0 0
-101-  0 0 0 0 1 0 0 0 0 0
0101-  0 0 0 1 0 0 0 0 0 0
-110-  0 0 0 0 1 0 0 0 0 0
1000-  1 0 0 0 0 0 0 0 0 0
.e
```

E. ESPRESSO OUTPUT

```
.na fsm
.ilb  SC InSt0* InSt1* InSt2* InSt3*
.ob  OutSt3* OutSt2* OutSt1* OutSt0* S3 S2 S1 S0 MUX_EN CLEAR
.i 5
.o 10
.p 20
00111 0001000000
00101 0110000000
00110 1110000000
1000- 1000000000
01-00 1001000000
0-011 0010000000
0-001 0100000000
0-010 1100000000
0-100 1010000000
-110- 0000100000
-011- 0000010000
-1-01 0000000100
-01-1 0000000100
010-- 0001000000
--011 0000000100
-101- 0000100011
-100- 0000011011
--0-1 0000000001
-0-1- 0000000011
--10- 0000001011
.e
```

APPENDIX B. MAGIC CELL LAYOUTS

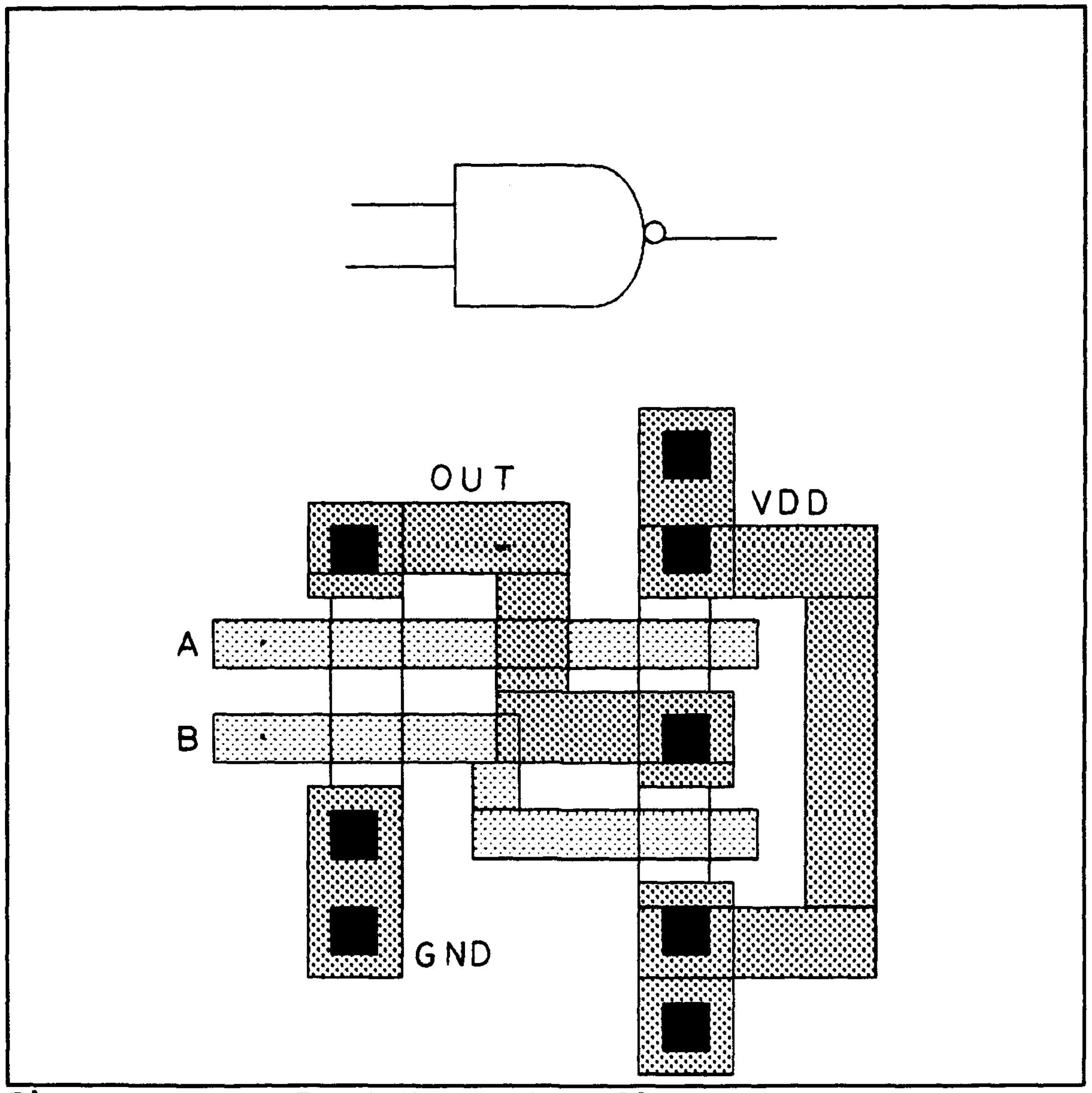


Figure 11. Two Input NAND Gate Cell Layout

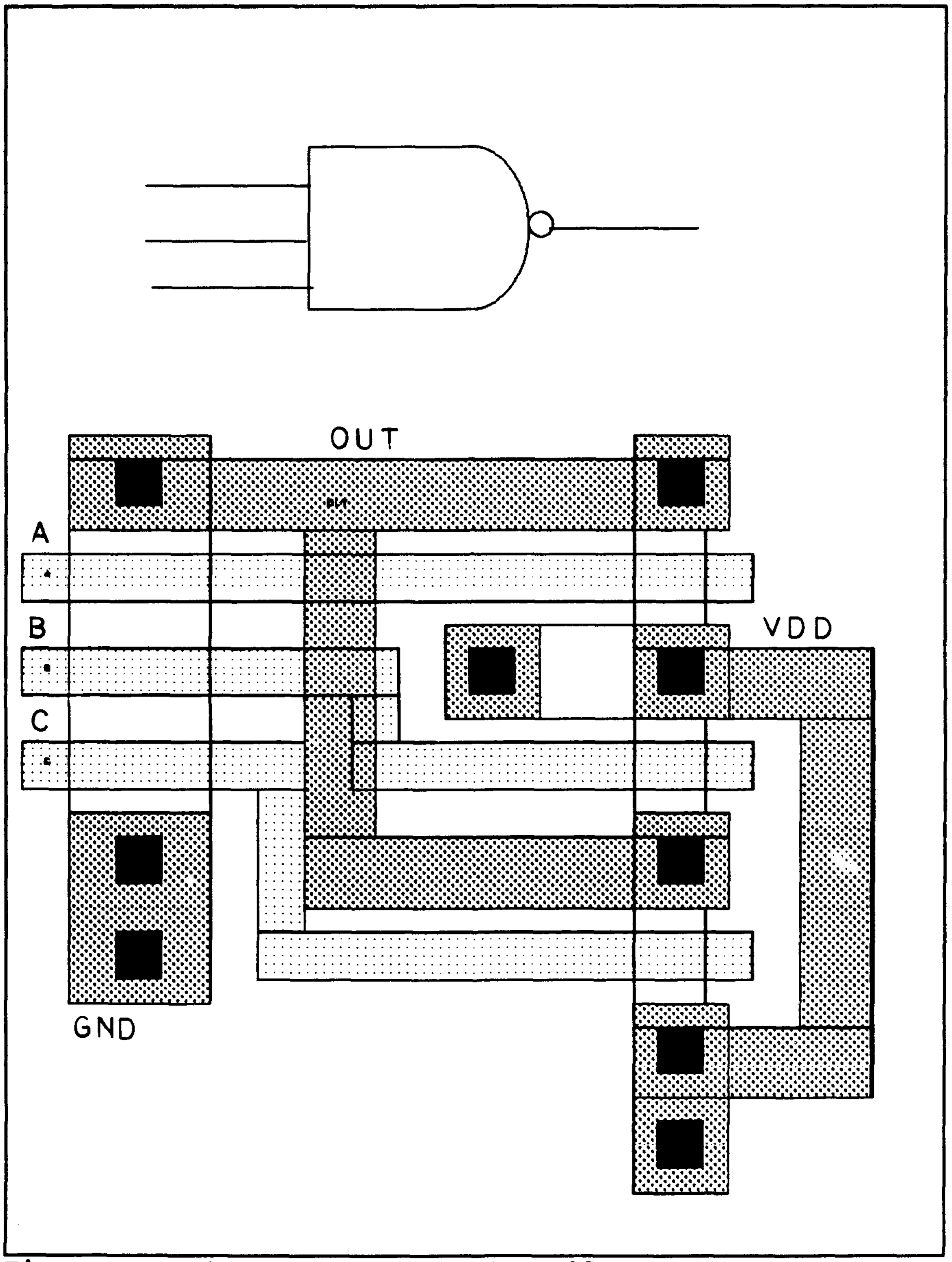


Figure 12. Three Input NAND Gate Cell Layout

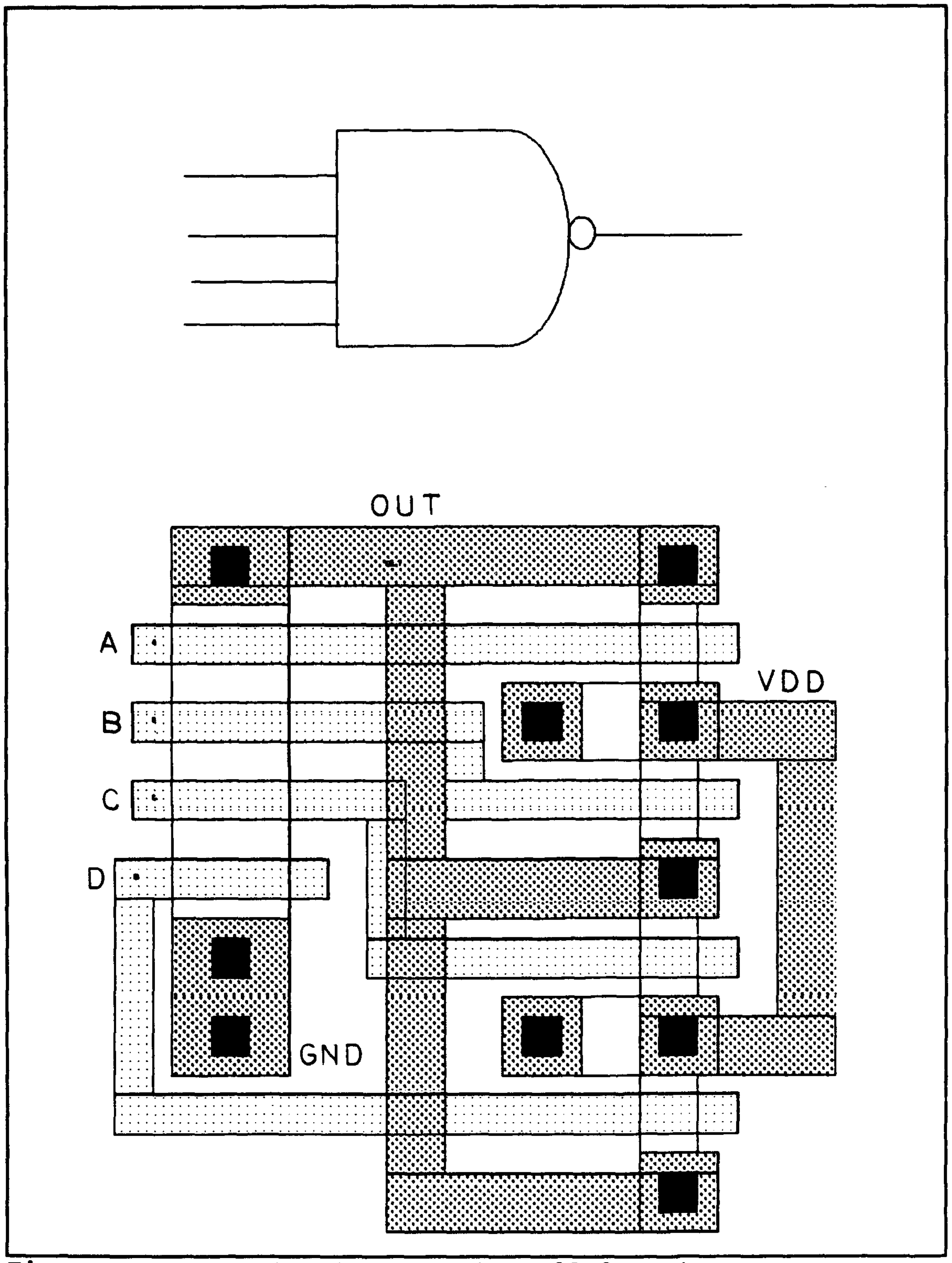


Figure 13. Four Input NAND Gate cell layout

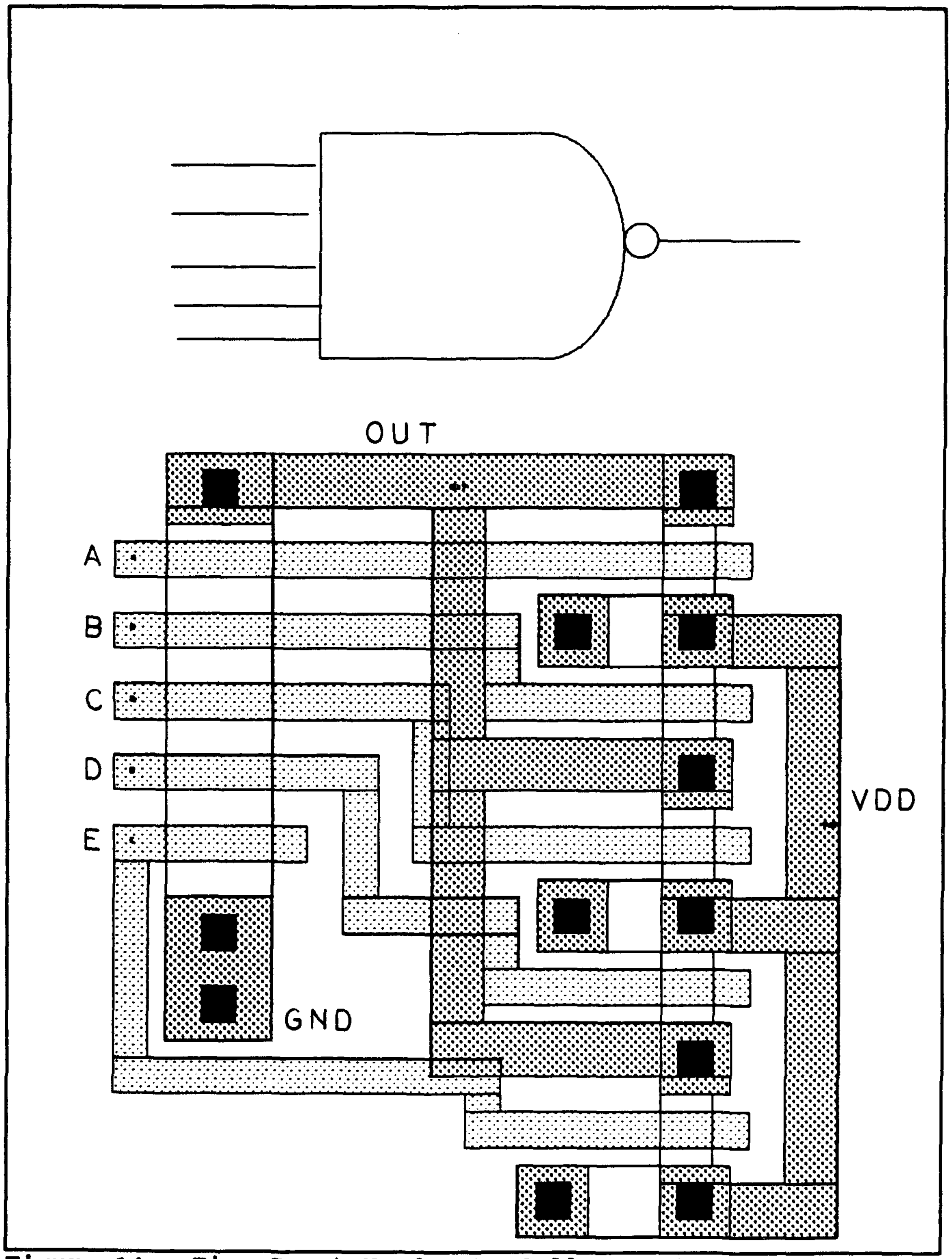


Figure 14. Five Input Nand Gate Cell Layout

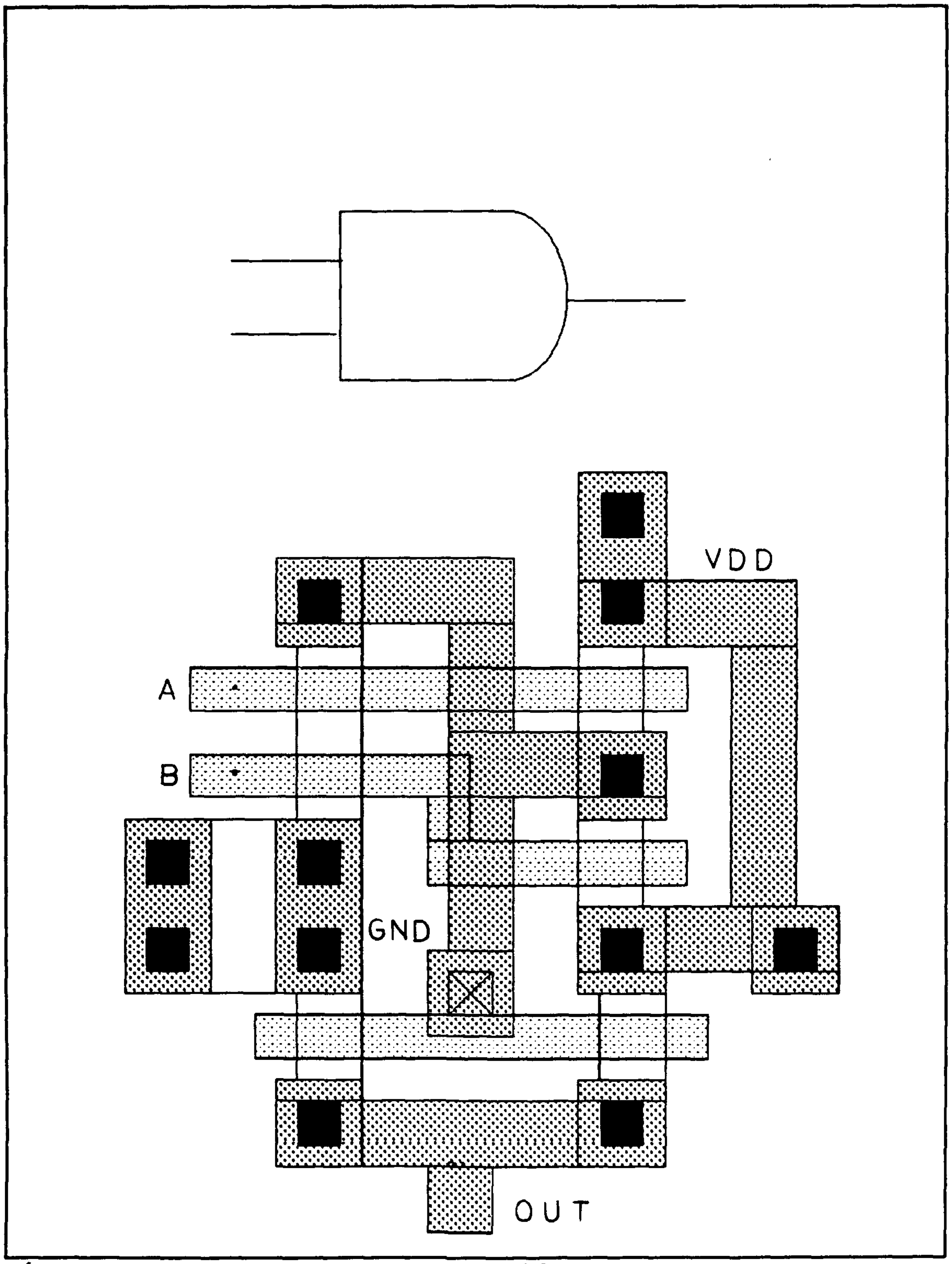


Figure 15. Two Input AND Gate Cell Layout

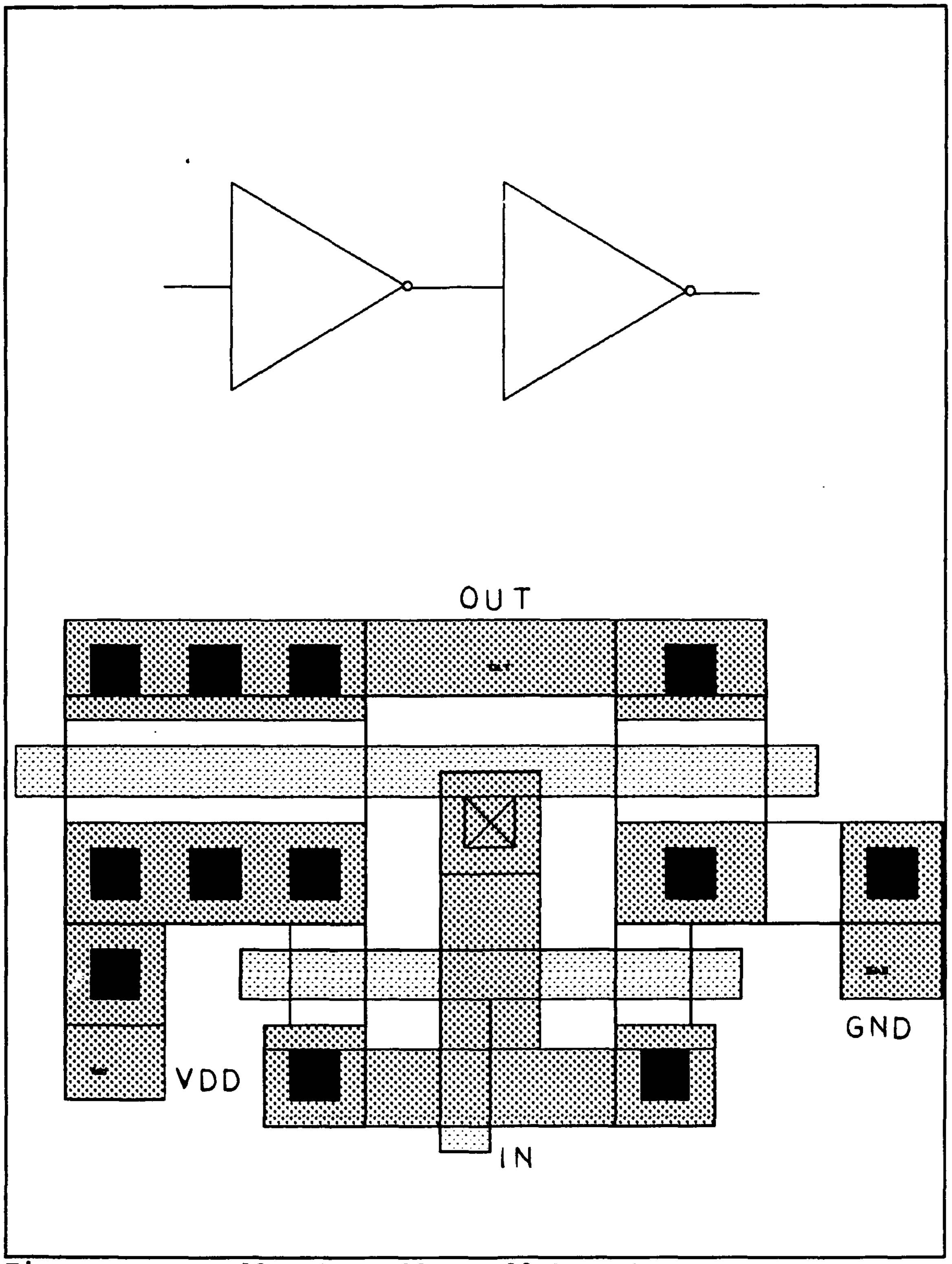


Figure 16. Small Data Buffer Cell Layout

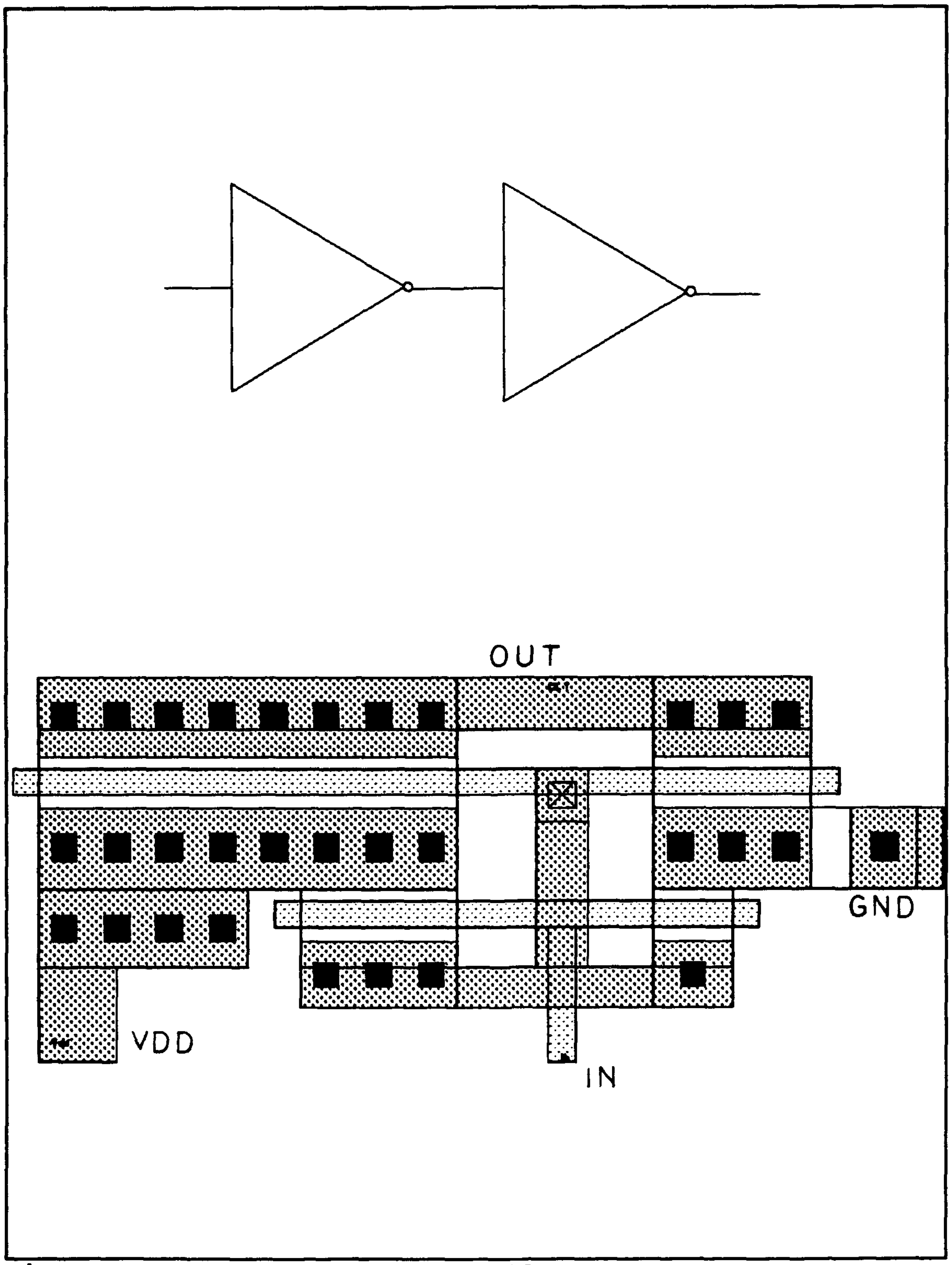


Figure 17. Large Data Buffer Cell Layout

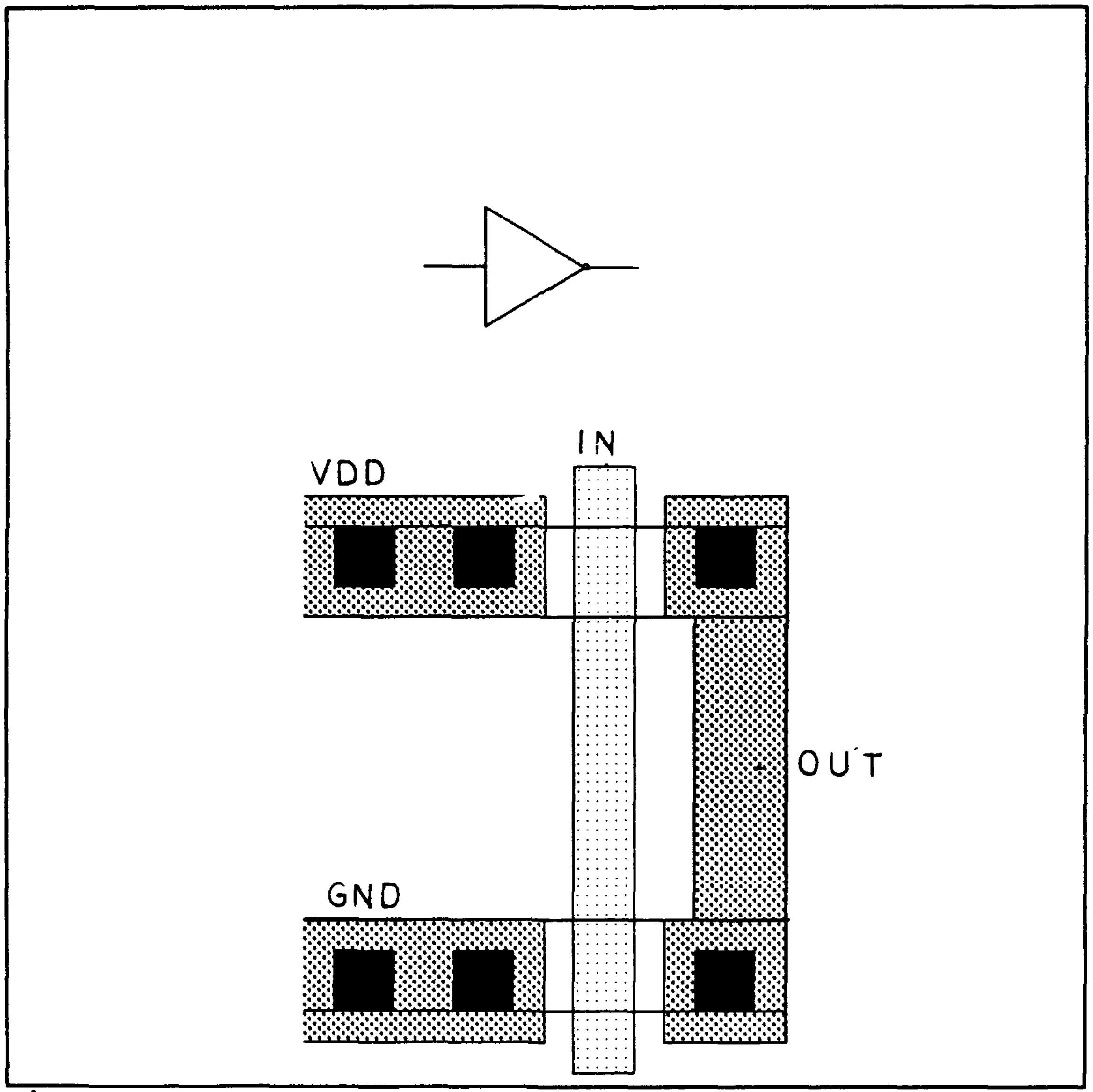


Figure 18. Small Inverter Cell Layout

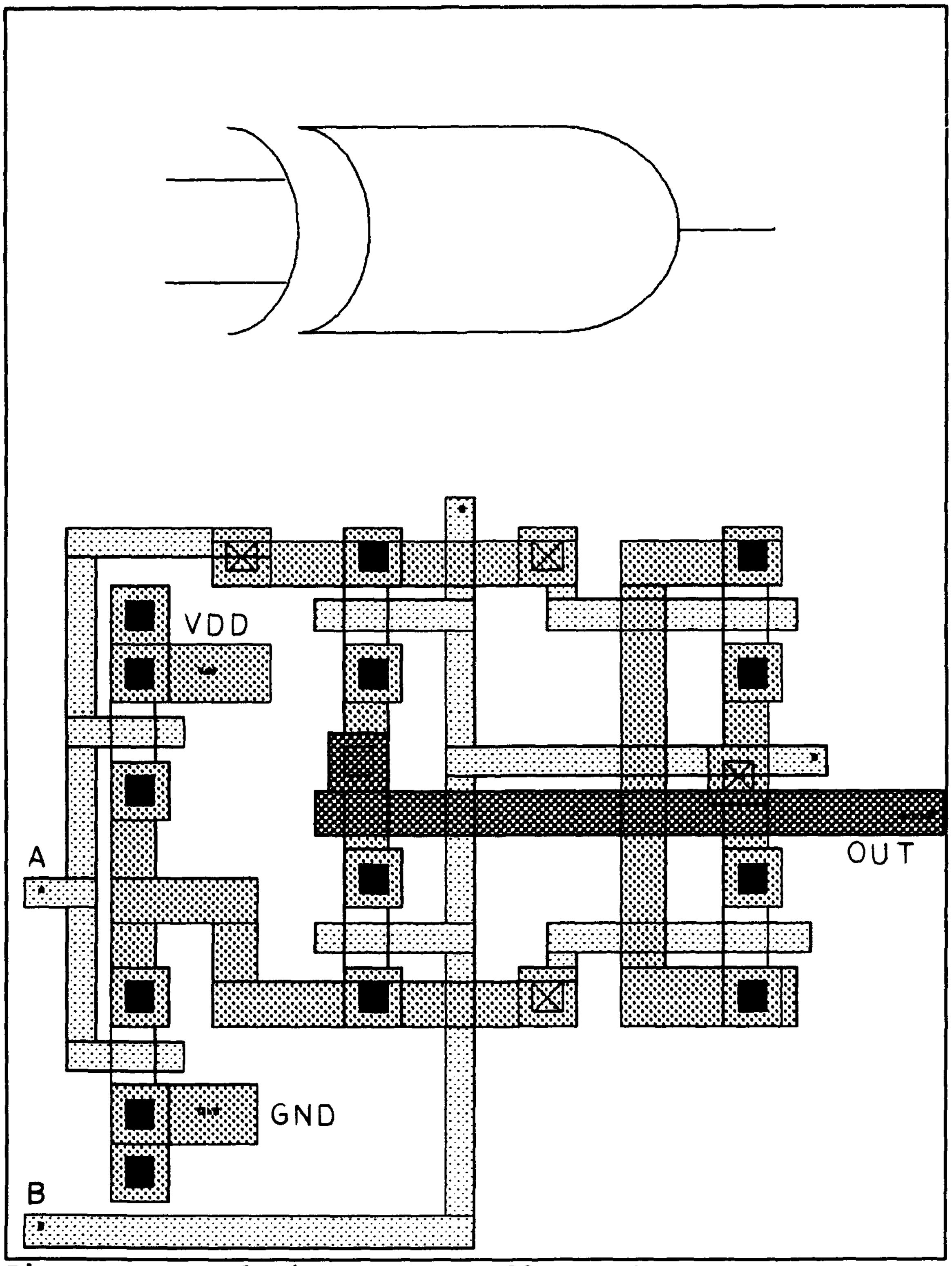


Figure 19. Exclusive-Or Gate Cell Layout

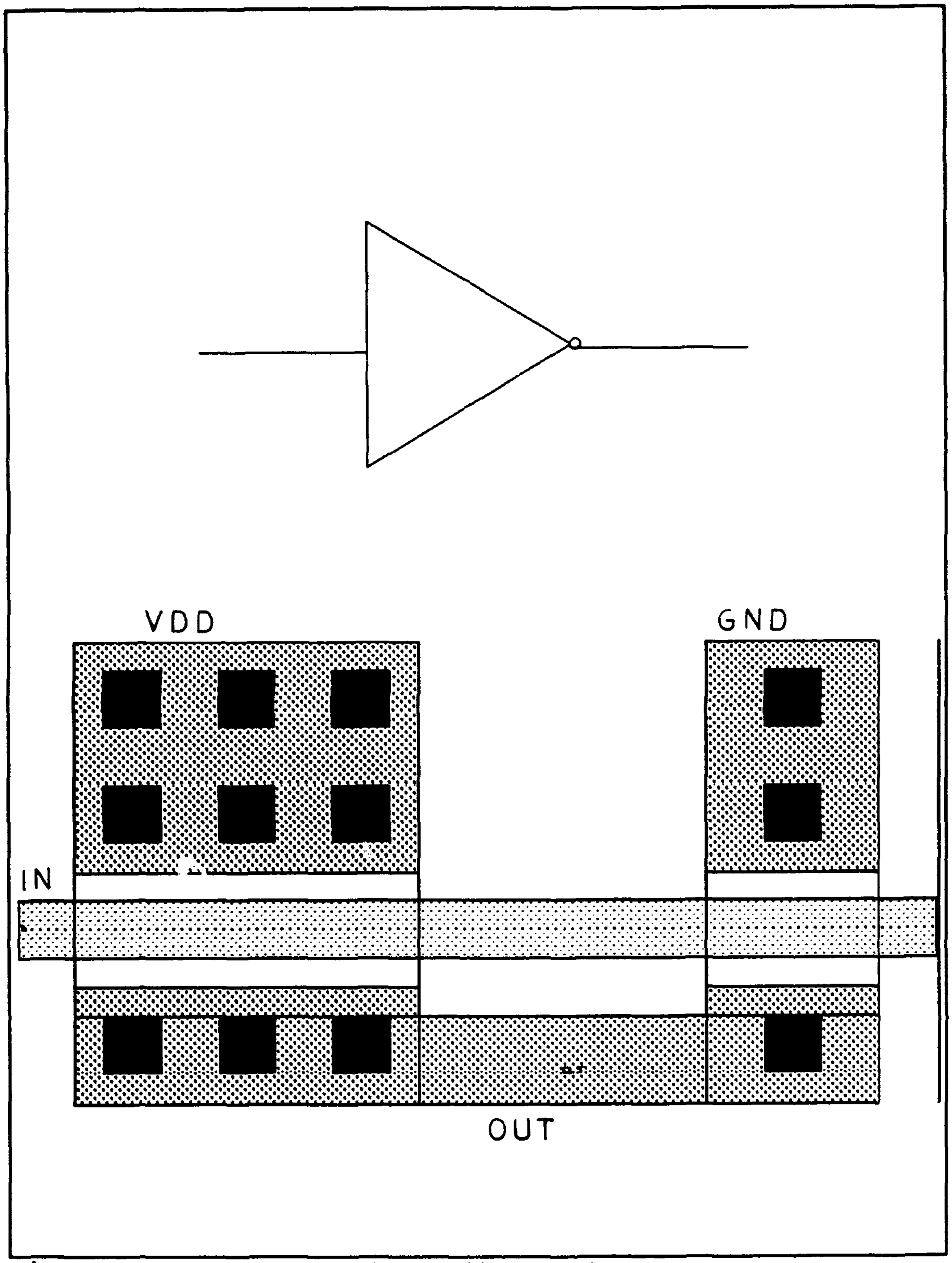


Figure 20. Large Inverter Cell Layout

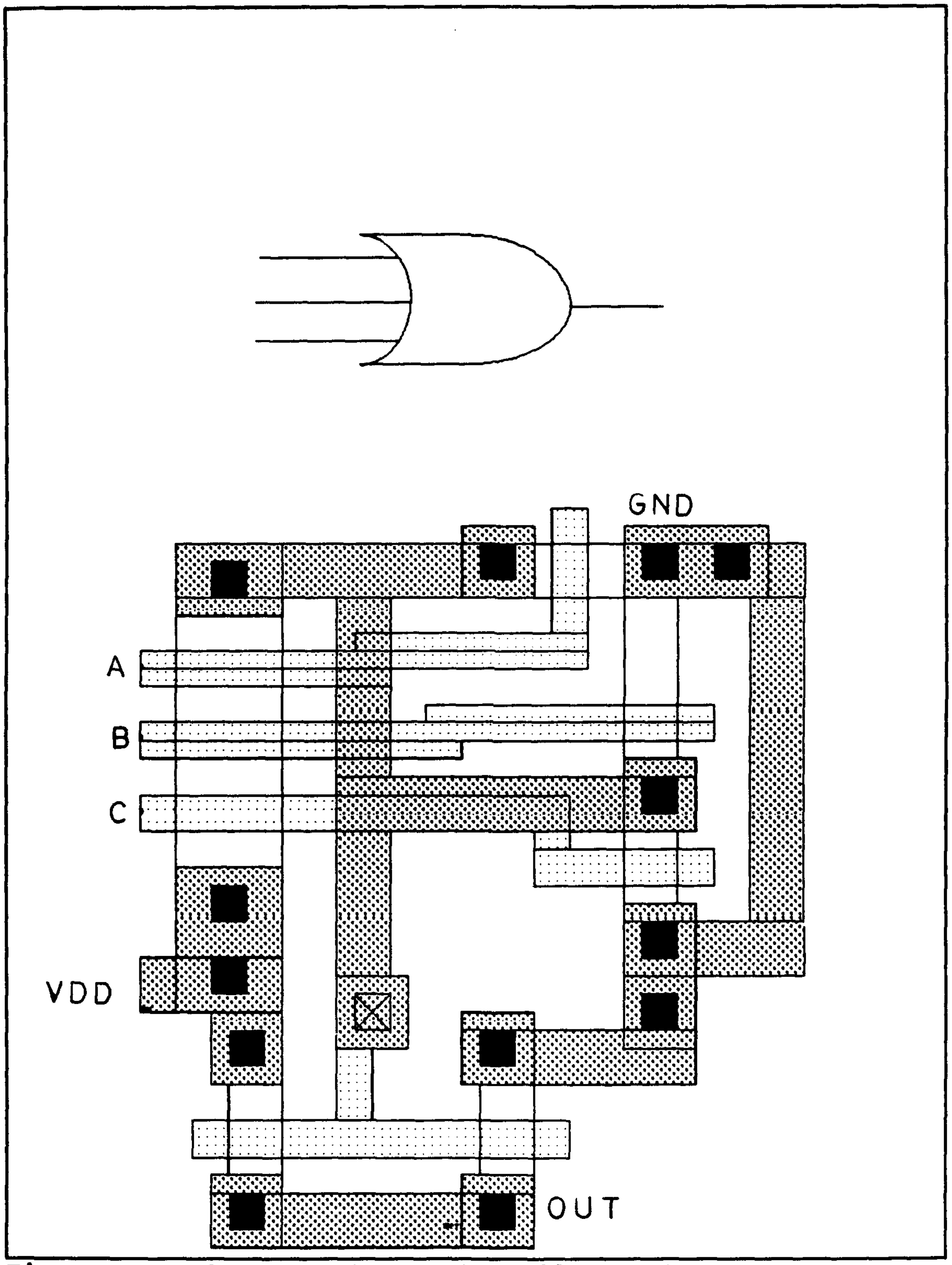


Figure 21. Three Input OR Gate Cell Layout

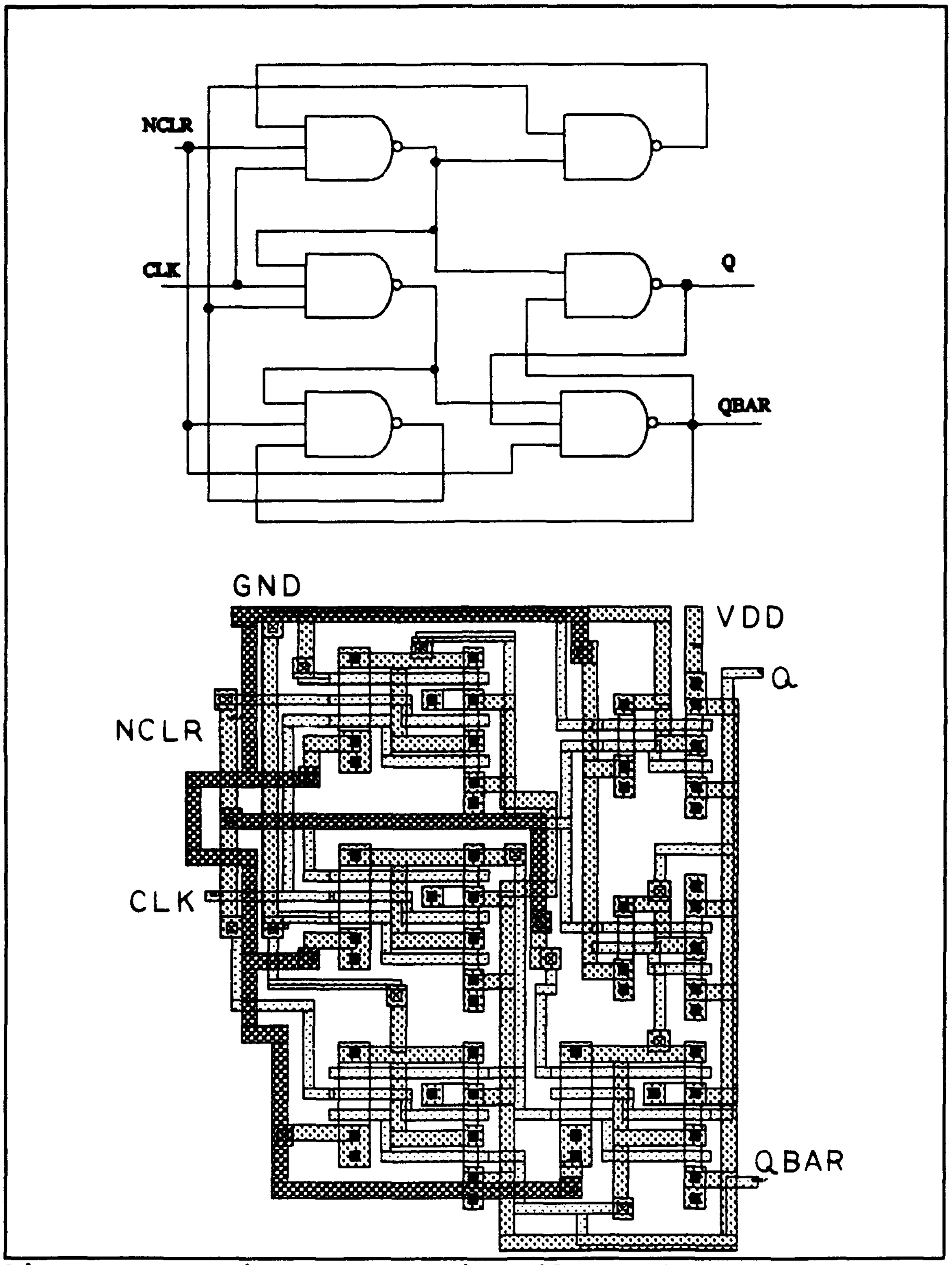


Figure 22. 1 Bit Counter Magic Cell Layout

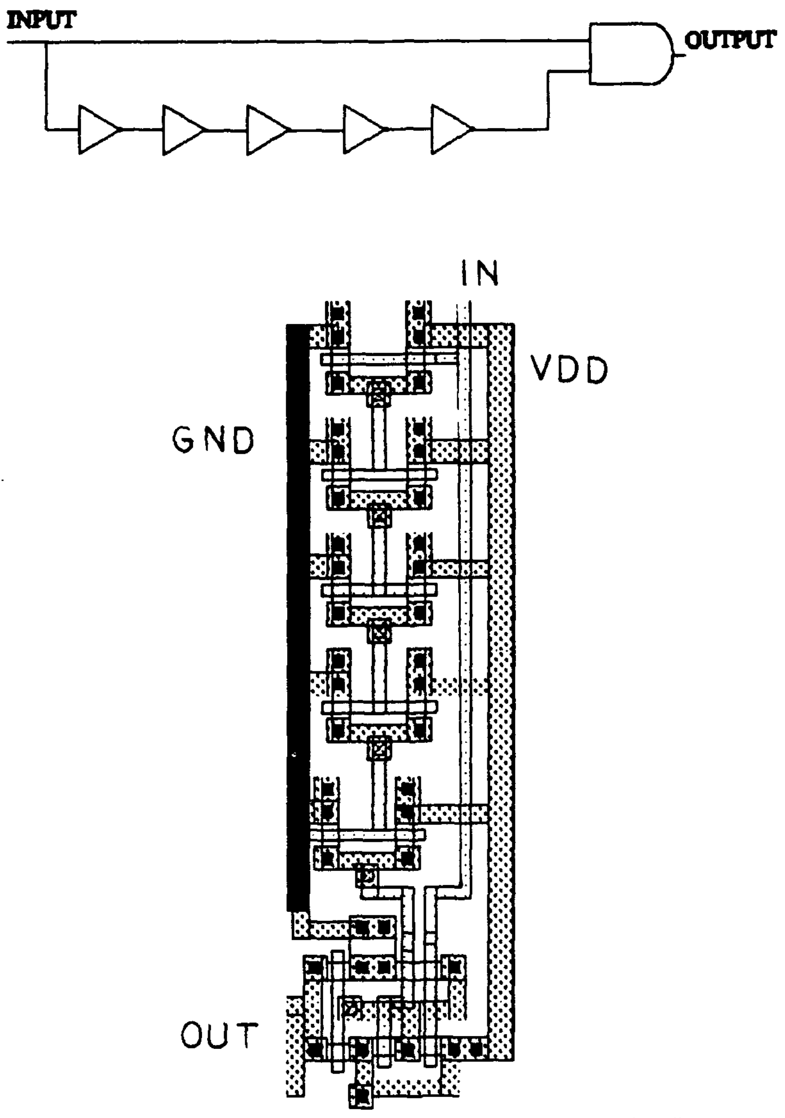
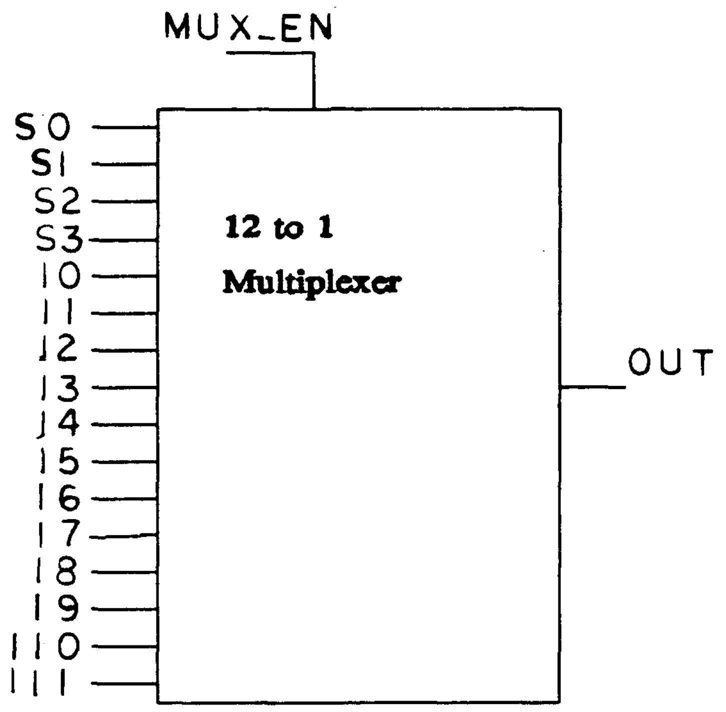


Figure 23. One Shot Magic Cell Layout



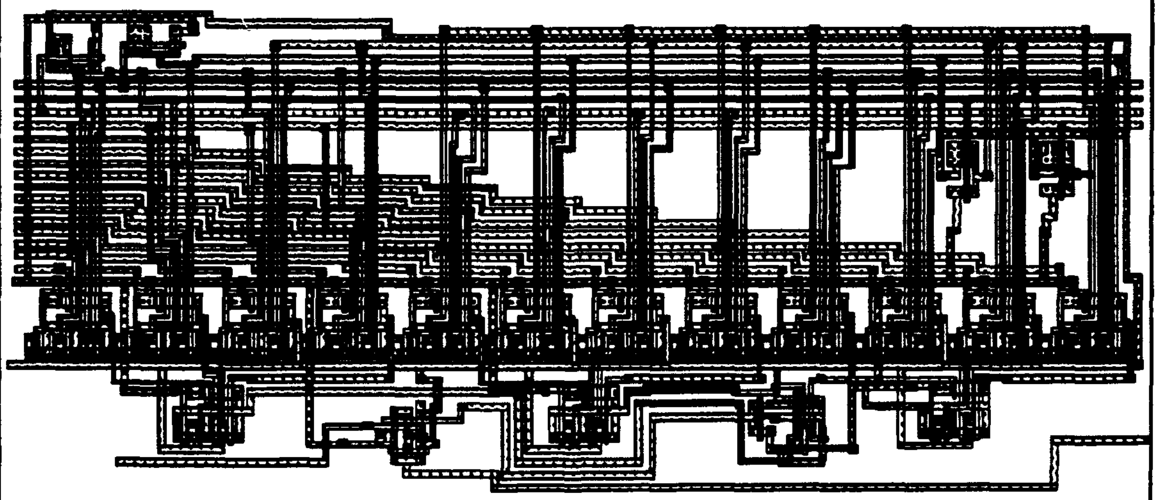


Figure 24. 12 Input To One Output Multiplexer Cell Layout

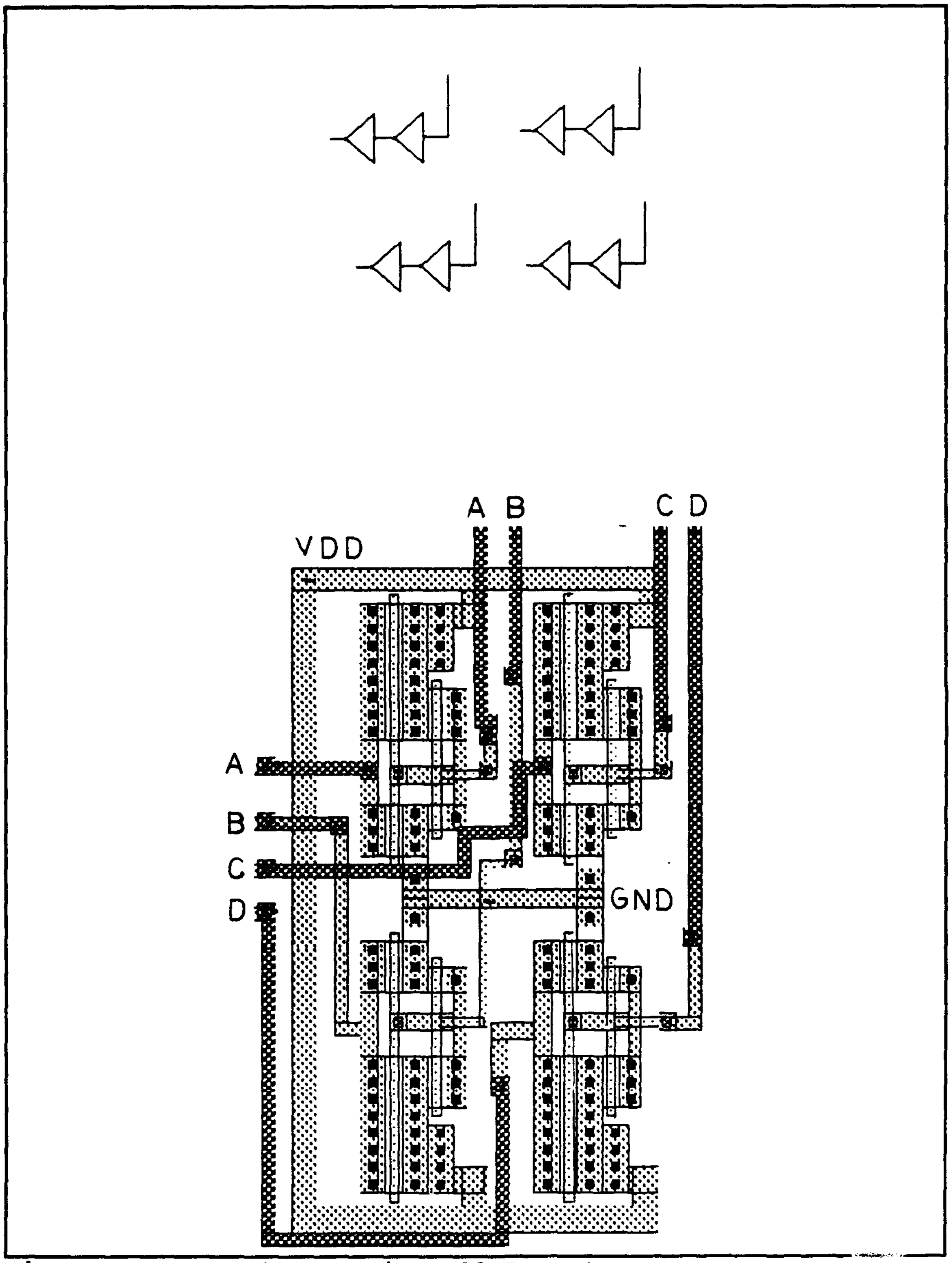


Figure 25. T-Buffer Magic Cell Layout

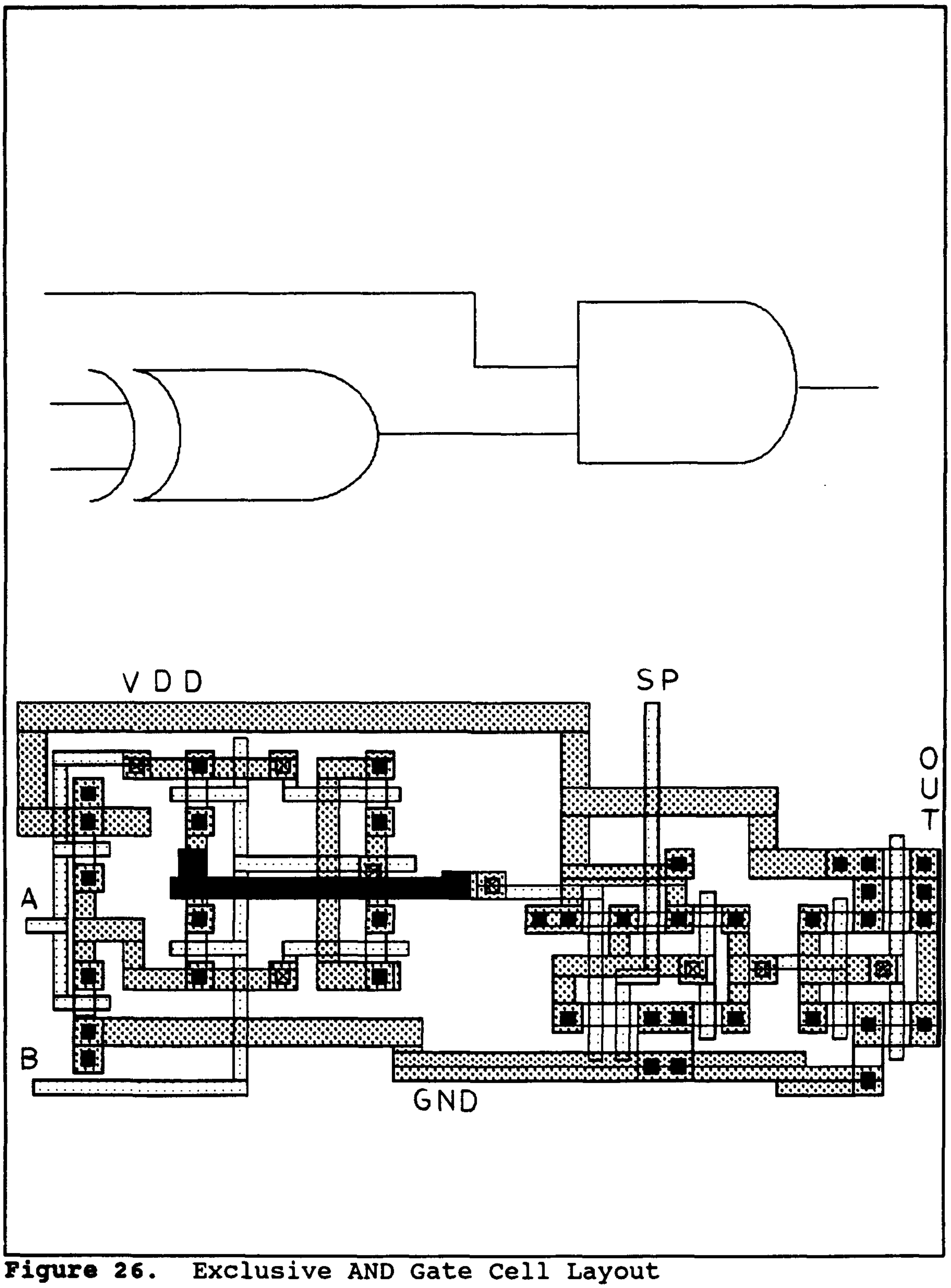


Figure 26. Exclusive AND Gate Cell Layout

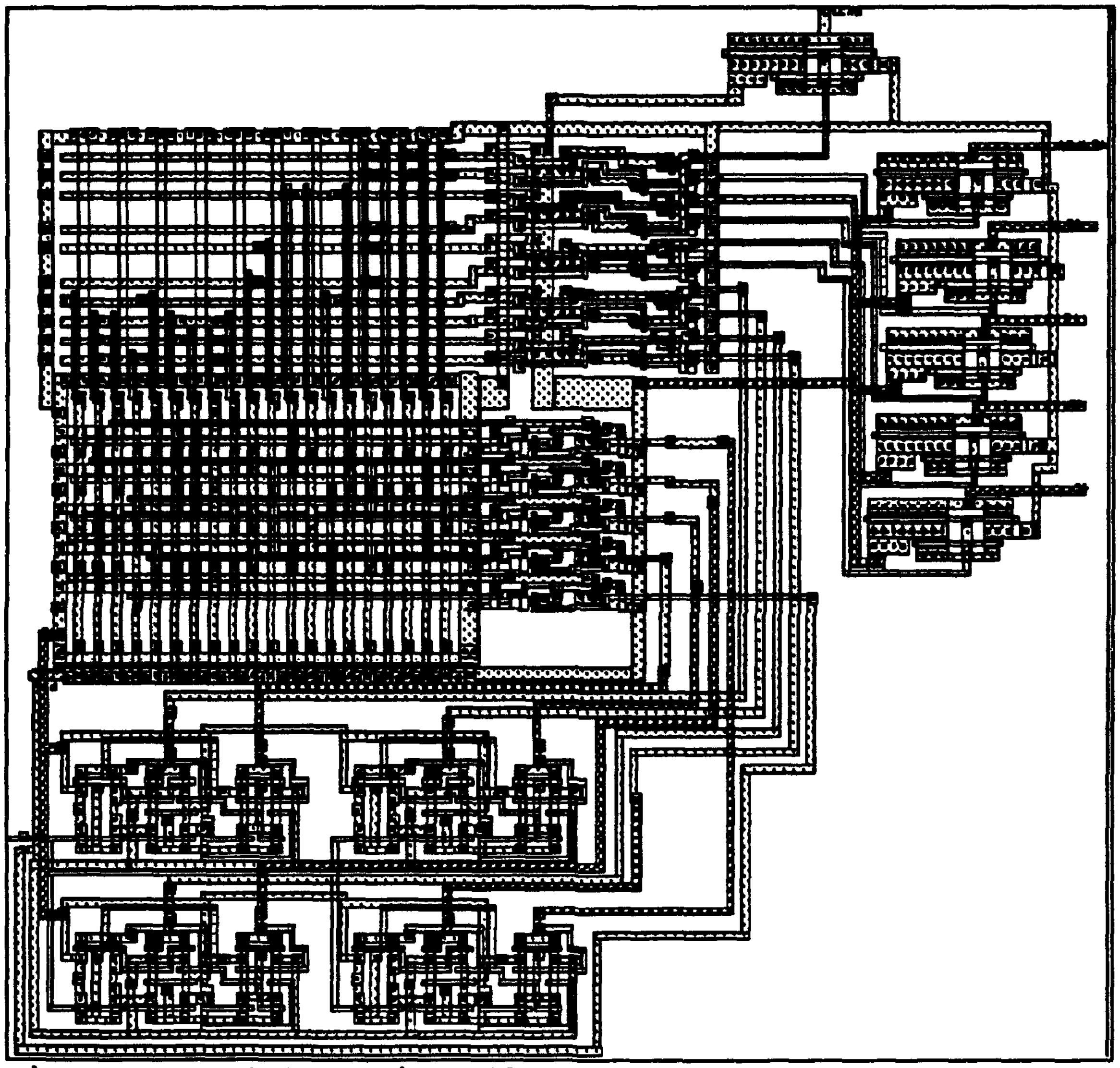


Figure 27. State Magic Cell Layout

APPENDIX C: SIMULATION DATA

A. FINITE STATE MACHINE SIMULATION

```
ESIM (V3.5 03/27/91)
247 transistors, 106 nodes (30 pulled up)
sim> w SC CLK CLEAR MUX_EN S0 S1 S2 S3
sim> V SC
1111000000000000000000000000000000000000000000000000
sim> V CLK
1010101010101010101010101010101010101010101010101010
sim> I
initialization took 218 steps
sim> I
initialization took 0 steps
sim> G
>1111000000000000000000000000000000000000000000000000:SC
>1010101010101010101010101010101010101010101010101010:CLK
>0011111111111111111111111111110000000000000000000000:CLEAR
>0000001111111111111111111111110000000000000000000000:MUX_EN
>0000000011001100110011001100110000000000000000000000:S0
>0000000000111100001111000011110000000000000000000000:S1
>0000000000000011111111000000000000000000000000000000:S2
>0000000000000000000000111111110000000000000000000000:S3
```

B. TWO-DIMENSIONAL HISTOGRAM CIRCUIT ESIM RUNS

Many simulations were completed to show correct operation of the complete chip. Each simulation consisted of 25 sampling pulses applied to a single bin. In each case, the simulation was run twice to verify proper setup of the circuit in the initial scan and correct counts received during subsequent cycles of the chip.

1. Bin 0 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  11111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MC  10101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 11111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MCA 10101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 0
V IN1 0
V IN2 0
V IN3 0
V IN4 0
V IN5 0
V IN6 0
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>11111111111111111111111111111111111111111111111111111100000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>11000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000011000000000000000000000000000:OD
>00000000000000000000000000000000000000000000000000000000011000000000000000000000000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>1111:1111111111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OA
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OD
>000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OE
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

2. Bin 1 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  111111111111111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MC  101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 111111111111111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MCA 101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 0
V IN2 0
V IN3 0
V IN4 0
V IN5 0
V IN6 0
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>111111111111111111111111111111111111111111111111111111111111111100000000000000000000000000000000:SC
>101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>000000000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OD
>000000000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OE
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>111111111111111111111111111111111111111111111111111111111111111100000000000000000000000000000000:SC
>101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>000000000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OA
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>000000000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OD
>000000000000000000000000000000000000000000000000000000000000000000001100000000000000000000000000:OE
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

3. Bin 2 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  111111111111111111111111111111111111111111111111111111111111000000000000000000000000000000
V MC  101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 111111111111111111111111111111111111111111111111111111111111000000000000000000000000000000
V MCA 101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 0
V IN3 0
V IN4 0
V IN5 0
V IN6 0
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>111111111111111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>000000000000000000000000000000000000000000000000000000000000000000110000000000000000000000:OD
>000000000000000000000000000000000000000000000000000000000000000000110000000000000000000000:OE
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>111111111111111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>000000000000000000000000000000000000000000000000000000000000000000110000000000000000000000:OA
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>000000000000000000000000000000000000000000000000000000000000000000110000000000000000000000:OD
>000000000000000000000000000000000000000000000000000000000000000000110000000000000000000000:OE
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

4. Bin 3 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MC  10101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MCA 10101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 0
V IN4 0
V IN5 0
V IN6 0
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000110000000000000000000:OD
>00000000000000000000000000000000000000000000000000000000000110000000000000000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000110000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000110000000000000000000:OD
>00000000000000000000000000000000000000000000000000000000000110000000000000000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

5. Bin 4 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  1111111111111111111111111111111111111111111111111100000000000000000000000000000
V MC  10101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 1111111111111111111111111111111111111111111111111100000000000000000000000000000
V MCA 10101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 0
V IN5 0
V IN6 0
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000011000000000000000000:OD
>00000000000000000000000000000000000000000000000000000000000011000000000000000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000011000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000011000000000000000000:OD
>00000000000000000000000000000000000000000000000000000000000011000000000000000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000U000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

6. Bin 5 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  1111111111111111111111111111111111111111111111111111111111000000000000000000000000000000
V MC  1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 1111111111111111111111111111111111111111111111111111111111000000000000000000000000000000
V MCA 1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 1
V IN5 0
V IN6 0
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>1111111111111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>0000000000000000000000000000000000000000000000000000000000000000000000110000000000000000:OD
>0000000000000000000000000000000000000000000000000000000000000000000000110000000000000000:OE
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>1111111111111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>0000000000000000000000000000000000000000000000000000000000000000000000110000000000000000:OA
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>0000000000000000000000000000000000000000000000000000000000000000000000110000000000000000:OD
>0000000000000000000000000000000000000000000000000000000000000000000000110000000000000000:OE
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

7. Bin 6 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  1111111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MC  1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 1111111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MCA 1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 1
V IN5 1
V IN6 0
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>1111111111111111111111111111111111111111111111111111111100000000000000000000000000000000:SC
>1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>0000000000000000000000000000000000000000000000000000000000000000000000001100000000000000:OD
>0000000000000000000000000000000000000000000000000000000000000000000000001100000000000000:OE
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>1111111111111111111111111111111111111111111111111111111100000000000000000000000000000000:SC
>1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>0000000000000000000000000000000000000000000000000000000000000000000000001100000000000000:OA
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>0000000000000000000000000000000000000000000000000000000000000000000000001100000000000000:OD
>0000000000000000000000000000000000000000000000000000000000000000000000001100000000000000:OE
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

8. Bin 7 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MC  10101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MCA 10101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 1
V IN5 1
V IN6 1
V IN7 0
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000110000000000:OD
>00000000000000000000000000000000000000000000000000000000000000000000110000000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000110000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000110000000000:OD
>00000000000000000000000000000000000000000000000000000000000000000000110000000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

9. Bin 8 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MC  101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 111111111111111111111111111111111111111111111111111100000000000000000000000000000000
V MCA 101010101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 1
V IN5 1
V IN6 1
V IN7 1
V IN8 0
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>111111111111111111111111111111111111111111111111111100000000000000000000000000000000:SC
>101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>000000000000000000000000000000000000000000000000000000000000000000000000110000000000:OD
>000000000000000000000000000000000000000000000000000000000000000000000000110000000000:OE
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>111111111111111111111111111111111111111111111111111100000000000000000000000000000000:SC
>101010101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>000000000000000000000000000000000000000000000000000000000000000000000000110000000000:OA
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>000000000000000000000000000000000000000000000000000000000000000000000000110000000000:OD
>000000000000000000000000000000000000000000000000000000000000000000000000110000000000:OE
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

10. Bin 9 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MC  10101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MCA 10101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 1
V IN5 1
V IN6 1
V IN7 1
V IN8 1
V IN9 0
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000001100000000:OD
>00000000000000000000000000000000000000000000000000000000000000000000001100000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000001100000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000001100000000:OD
>00000000000000000000000000000000000000000000000000000000000000000000001100000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0I
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0J
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0K
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0L
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0M
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0N
>00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0O
>000000000000000C000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000:0P
```

11. Bin 10 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MC  10101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MCA 10101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 1
V IN5 1
V IN6 1
V IN7 1
V IN8 1
V IN9 1
V IN10 0
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000000011000000:OD
>00000000000000000000000000000000000000000000000000000000000000000000000011000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000011000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000000011000000:OD
>00000000000000000000000000000000000000000000000000000000000000000000000011000000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

12. Bin 11 simulation and results

```
w SC MC OA OB OC OD OE OF OG OH OI OJ OK OL OM ON OO OP
V SC  11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MC  10101010101010101010101010101010101010101010101010101010101010101010101010101010
V SCA 11111111111111111111111111111111111111111111111111000000000000000000000000000000
V MCA 10101010101010101010101010101010101010101010101010101010101010101010101010101010
V IN0 1
V IN1 1
V IN2 1
V IN3 1
V IN4 1
V IN5 1
V IN6 1
V IN7 1
V IN8 1
V IN9 1
V IN10 1
I
I
I
I
I
I
I
I
G
10270 transistors, 4986 nodes (61 pulled up)
initialization took 31027 steps
initialization took 7836 steps
initialization took 5974 steps
initialization took 7037 steps
initialization took 9753 steps
initialization took 518 steps
initialization took 0 steps
initialization took 0 steps
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000000000110000:OD
>00000000000000000000000000000000000000000000000000000000000000000000000000110000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
10270 transistors, 4986 nodes (61 pulled up)
sim> G
>11111111111111111111111111111111111111111111111111000000000000000000000000000000:SC
>10101010101010101010101010101010101010101010101010101010101010101010101010101010:MC
>00000000000000000000000000000000000000000000000000000000000000000000000000110000:OA
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OB
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OC
>00000000000000000000000000000000000000000000000000000000000000000000000000110000:OD
>00000000000000000000000000000000000000000000000000000000000000000000000000110000:OE
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OF
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OG
>00000000000000000000000000000000000000000000000000000000000000000000000000000000:OH
```

```
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OI
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OJ
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OK
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OL
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OM
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:ON
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OO
>0000000000000000000000000000000000000000000000000000000000000000000000000000000000:OP
```

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